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SECTION 1

1

OPERATIONAL AMPLIFIERS

James Bryant, Walt Kester

This section describes operational amplifiers and discusses their structure and specifications. It is hard to decide which to discuss first, since discussion of specifications, to be useful, entails reference to structures, and discussion of structures likewise requires reference to the performance feature that they are intended to optimize.

Since the majority of readers will have at least some familiarity with operational amplifiers and their specifications, we shall discuss structures first, and assume that readers will have at least a first-order idea of the definitions of the various specifications. Where this assumption proves ill-founded, the reader should look ahead to verify any definitions required.

OPERATIONAL AMPLIFIERS

- Structure and Specifications are Interdependent
- In this section, we look at
 - ◆ Structures First: Input and Output
- THEN
- ◆ Specifications

Figure 1.1

DEFINITION OF AN OP AMP

An Operational Amplifier (hereafter referred to as an "op amp") is an amplifier with a differential input having high common-mode rejection, and high, but not particularly stable or well-defined, differential gain. In most applications, its closed loop gain is stabilized by large amounts of negative feedback. Op amps have positive and negative supplies, but few, if any, have a ground connection, so the output does not have its own reference potential.

In the past, high precision op amps have sometimes been referred to as

"instrumentation grade" op amps, but this term can give rise to misunderstandings and should be discouraged. An instrumentation amplifier (hereafter referred to as an "in-amp") is not an op amp (see Figure 1.2). An in-amp, like an op amp, has a high impedance differential input with high common-mode rejection, but its gain is *accurately defined* without the need for an external network to provide the negative feedback to its inputs. Almost all in-amps have an output voltage reference pin.

THE OP AMP IS NOT AN INSTRUMENTATION AMP

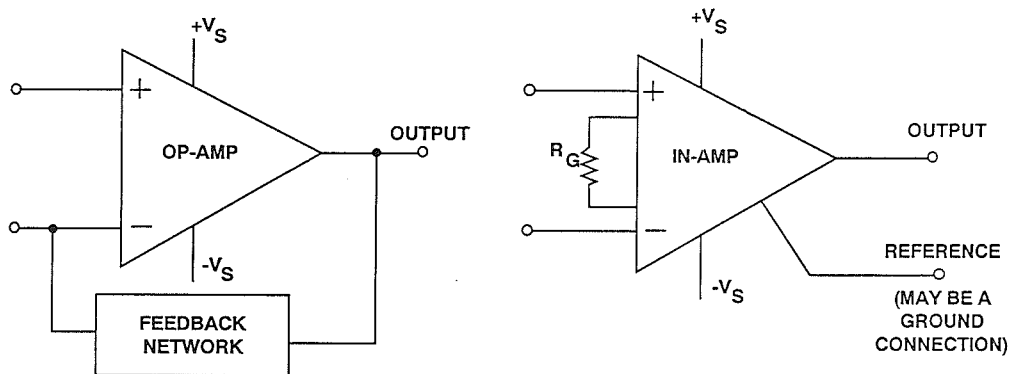


Figure 1.2

The most common type of in-amp is made with three op-amps and seven precision resistors as shown in Figure 1.3. In the past, a common use of quad op amps was the construction of in-amps, but today it is cheaper to use an IC in-amp. The performance of an in-amp is critically dependent on the

matching of its resistors. For instance, if a common mode rejection ratio (CMRR) of only 80 dB is required, the cost of the necessary 0.01% ratio-matched resistors will be much greater than the cost difference between an IC in-amp with on-chip trimmed resistors and a quad op amp.

THREE OP-AMP INSTRUMENTATION AMP

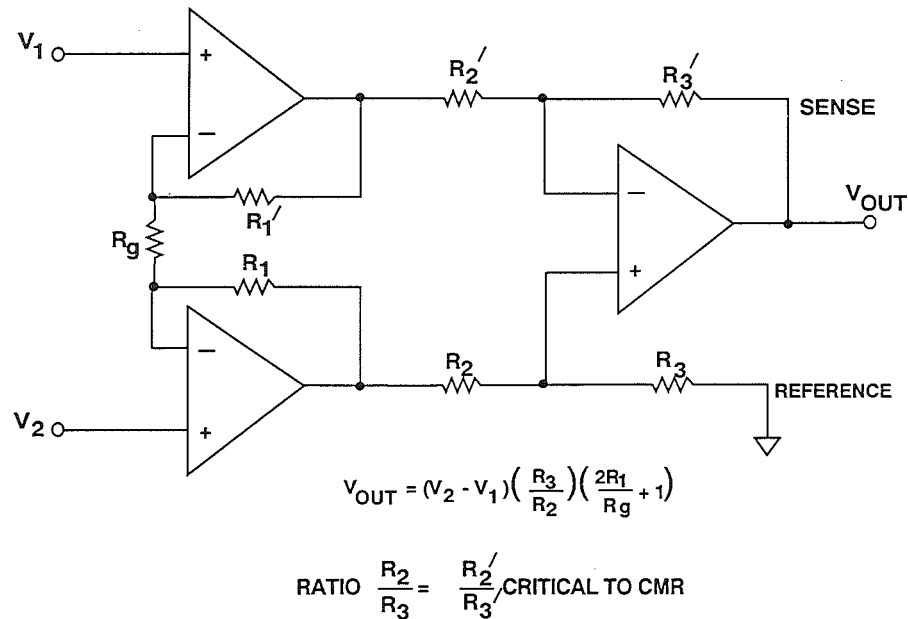


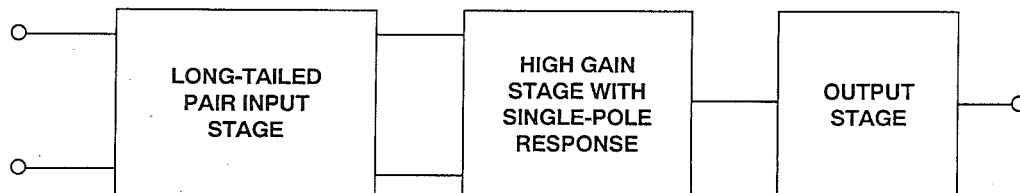
Figure 1.3

STRUCTURE OF CLASSICAL (VOLTAGE FEEDBACK) OP AMPS

The first operational amplifiers were manufactured in the 1940s and 1950s and used thermionic valves (vacuum tubes), but their basic structure was essentially similar to modern voltage feedback op amps and is shown in Figure 1.4. The input stage consisted of

a long-tailed pair (a differential input/differential output structure having good common-mode rejection). There was then a high gain stage with a single pole frequency response, and finally a single-ended output stage.

VOLTAGE FEEDBACK OP AMP STAGES



MODEL

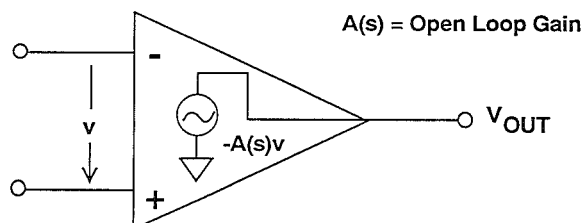


Figure 1.4

The op amp's gain to the differential input voltage, v , is its *open loop voltage gain* $A(s)$. $A(s)$ is a dimensionless quantity and is expressed as number or in dB. $A(s)$ is usually a large quantity (in most cases 100,000 or greater) and is a function of frequency. The op amp operating in the open loop mode as shown in Figure 1.4 is not very useful (except, under certain conditions, as a comparator). A small amount of input voltage will cause the output of the op

amp to swing to one of the supply rails (depending on the input polarity) and saturate. By applying negative feedback from the output of the op amp to the inverting input using a feedback network, we create the classical *closed loop* configurations shown in Figure 1.5. We will now define some important parameters associated with feedback circuits: *feedback factor*, *noise gain*, and *loop gain* (see Reference 1).

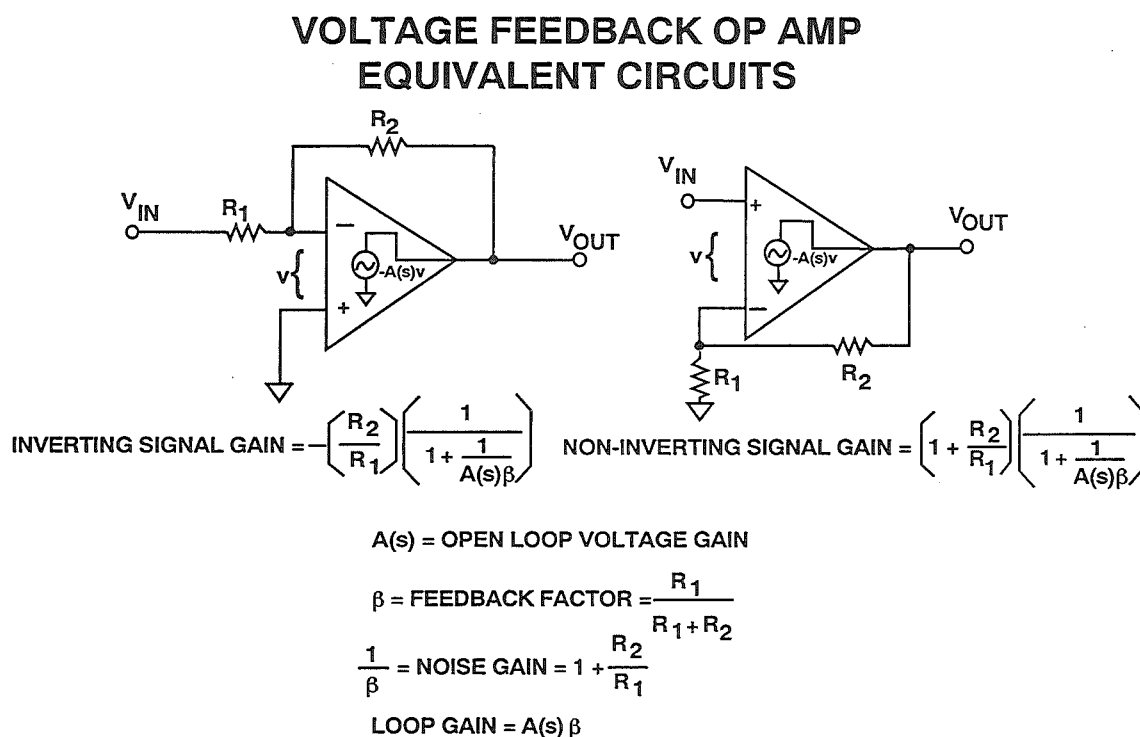


Figure 1.5

The *feedback factor* is the ratio of the output signal to the signal fed back to the inverting input and is given by

$$\beta = \frac{R_1}{R_1 + R_2}$$

The reciprocal of the feedback factor is the *noise gain* of the circuit. It is called this because it represents the voltage

gain to the output of a voltage noise source in series with the op amp input terminals.

$$\text{Noise Gain} = \frac{1}{\beta} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$$

Notice that the signal fed back from the output is attenuated by the feedback factor β and is then amplified by $A(s)$. The total gain of the loop is $A(s)\beta$, or the

loop gain. The loop gain is a measure of how closely the amplifier approaches the ideal. This can be seen by examining the closed-loop signal gain expressions in Figure 1.5. In the case of the inverting mode,

$$\text{Signal Gain} = -\frac{R_2}{R_1} \left(\frac{1}{1 + A(s)\beta} \right)$$

The greater the loop gain, $A(s)\beta$, the closer the op amp is to ideal performance. In an ideal op amp, $A(s) = \infty$, and the signal gain is $-R_2/R_1$. In practice, either a greater $A(s)$ or a greater β (more feedback) maximizes $A(s)\beta$.

It is the value of the loop gain at a specified frequency which will determine the overall accuracy of the op amp at that frequency. As the frequency increases, the loop gain decreases, causing a loss of accuracy and linearity.

If the op amp has a single-pole open-loop gain response and gain is plotted in dB versus the logarithm of the frequency, then the open-loop gain decreases at a rate of 6dB/octave starting at the corner frequency defined by the pole. The loop gain $A(s)\beta$ decreases at the same rate.

Since the gain stage is embedded in the amplifier, it is rarely of concern to the end-user, so we shall mainly be concerned with the input and output stages. All classical voltage feedback op amps use a long-tailed pair as an input stage. Its basic structure is a pair of matched amplifying devices, current fed in their joined cathodes (or emitters or sources), with the differential input applied to their grids (or bases or gates), with the output appearing as a differential current in their anodes (or collectors or drains) (see Figure 1.6).

A TYPICAL OLD FASHIONED LONG-TAILED PAIR

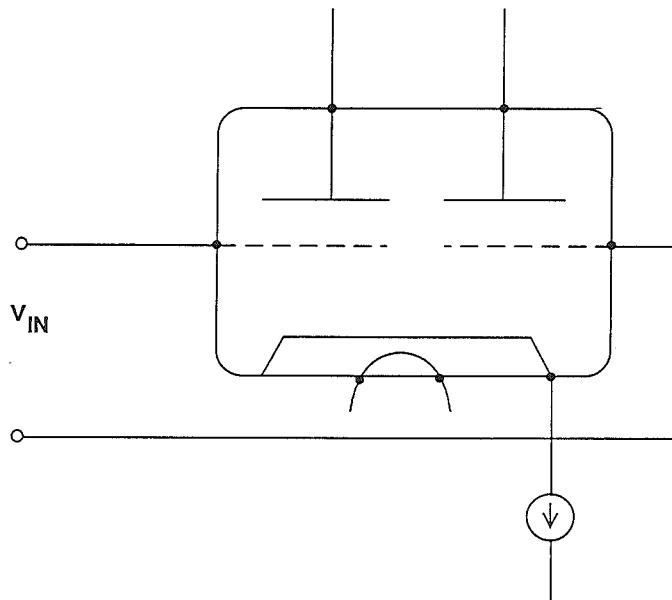


Figure 1.6

Since valves (tubes) are rarely used today, we shall consider the structures used in monolithic op amps, starting

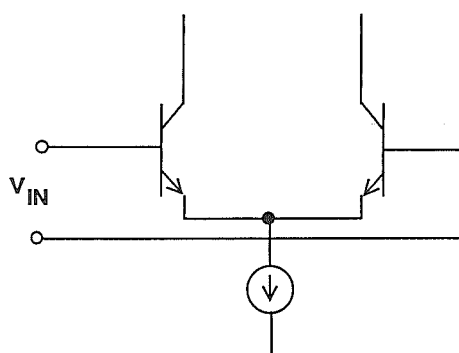
with the simple bipolar transistor input stage.

Bipolar Input Stage

The basic bipolar input stage shown in Figure 1.7 consists of a long-tailed pair built with bipolar transistors. It has a number of advantages: it is simple, has very low offset, the bias currents in the inverting and non-inverting inputs are well-matched and do not vary greatly with temperature, and minimizing the

initial offset voltage of a bipolar op amp by laser trimming also minimizes its drift over temperature. This architecture is used by the earliest monolithic op amps such as the $\mu A709$, as well as some modern high-speed types like the AD817.

BIPOLAR TRANSISTOR INPUT STAGE



- Low Offset: As Low as $10\mu V$
- Low Offset Drift: As Low as $0.1\mu V/^{\circ}C$
- Temperature Stable I_{bias}
- Well-Matched Bias Currents
- Low Voltage Noise: As Low as $1nV/\sqrt{Hz}$
- High Bias Currents: $50nA - 10\mu A$
- (Except Super-Beta: $50pA - 5nA$, More Complex and Slower)
- Medium Current Noise: $1pA/\sqrt{Hz}$

Figure 1.7

The input bias current is the base current of the long-tailed pair. It can be quite high, especially in high speed amplifiers, because the collector currents are high. The current noise of a bipolar input op amp is not particularly low.

The bias current of a simple bipolar input stage may be reduced by using *super-beta* transistors. These are devices with a very narrow base region

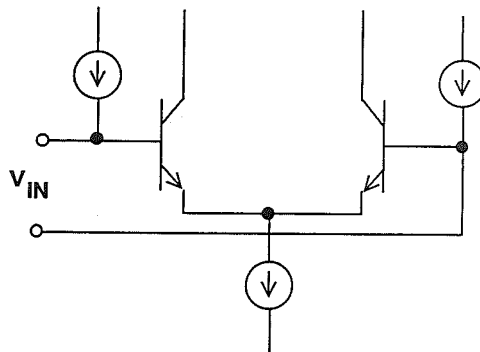
and a current gain of thousands or tens of thousands, rather than the more usual hundreds. Operational amplifiers with super-beta input stages have lower bias currents, but they have limited frequency response. Since the breakdown voltages of super-beta devices are quite low, they require additional circuitry to protect the input stage from damage caused by over-voltage. The AD705 and OP-97 are typical high performance super-beta op amps.

Bipolar Bias Current Compensated Input Stage

The simple bipolar input stage exhibits high bias current because the bias currents are the base currents of the input transistors. If we provide the necessary bias current by means of a current source at each input (see Figure 1.8), the only *external* current flowing in

the input terminals is the difference current between the base current and the current source. This can be quite small. The well-known OP-07 and all its family are examples of bias compensated op amps.

BIAS-CURRENT COMPENSATED BIPOLAR INPUT



- Low Offset Voltage: As Low as $10\mu\text{V}$
- Low Offset Drift: As Low as $0.1\mu\text{V}/^\circ\text{C}$
- Temperature Stable I_{bias}
- Low Bias Currents: $< 0.5 - 10\text{nA}$
- Low Voltage Noise: As Low as $1\text{nV}/\sqrt{\text{Hz}}$
- Poor Bias Current Match (Currents May Even Flow in Opposite Directions)
- High Current Noise
- Not Very Useful at HF

Figure 1.8

Bias current compensated input stages have many of the good features of the simple bipolar input stage: low voltage noise, low offset, and low drift. Additionally, they have low bias current which is fairly stable with temperature. However, their current noise is not very good, and their bias current matching is poor. These features result from the external bias current being the *difference* between the current source and the input transistor base current. Both of these currents inevitably have noise. Since they are uncorrelated, the two noises add (root sum of squares), even though the currents subtract.

Since the external bias current I_b is the difference between two nearly equal currents, there is no particular reason why the net current should have any particular polarity, so the bias currents of bias-compensated op amps may not only be mismatched, they may actually flow in opposite directions! In most applications this is not important, but in some it can have unexpected effects (for example the droop of a sample-and-hold (SHA) built with a bias-compensated op amp may have either polarity).

FET Input Stages

Field-Effect Transistors (FETs) have much higher input impedance than bipolar junction transistors (BJTs) and would therefore seem to be ideal devices for op amp input stages. However, they cannot be manufactured on all bipolar IC processes, and when a process allows their manufacture, they have their own problems.

FETs have high input impedance, low bias current, and good high frequency performance (the lower g_m of the FET devices allows higher tail currents, thereby increasing the slew rate of the op amp). FETs also have low current

noise. The offset of FET long-tailed pairs, however, is not as good as the offset of BJTs, and trimming for minimum offset does not minimize drift. A separate trim is needed for drift, and as a result, offset and drift in a JFET op amp, while good, are not as good as the best BJT ones (see Figure 1.9). It is possible to make JFET op amps with very low voltage noise, but the devices involved are very large and have quite high input capacitance, which varies with input voltage, and so a trade-off is involved between voltage noise and input capacitance.

JUNCTION FIELD EFFECT TRANSISTOR (JFET) INPUT OP AMP STAGE SHOWING OFFSET AND DRIFT TRIMS

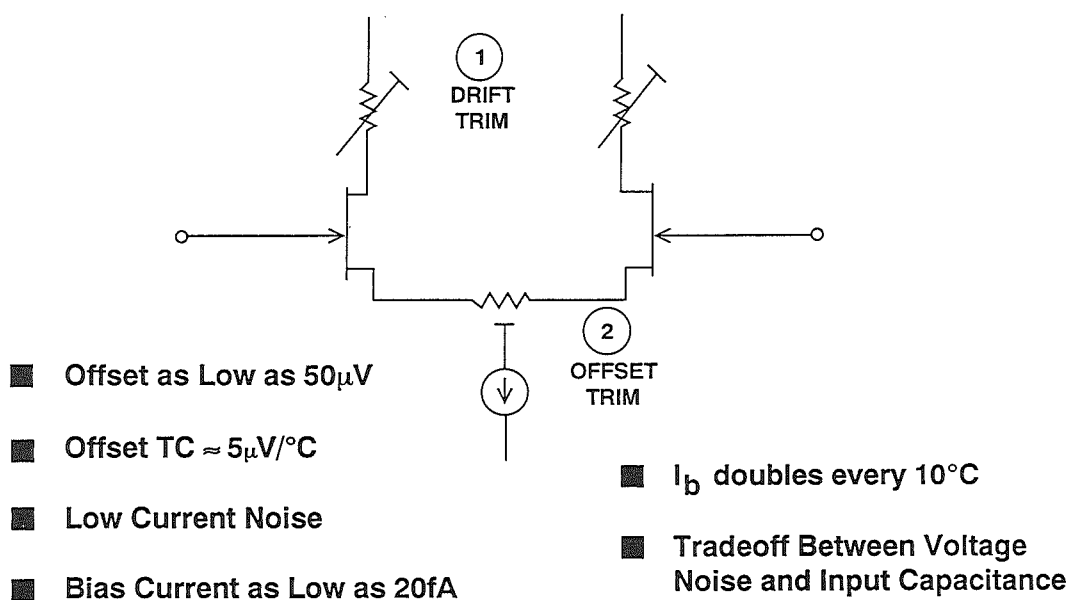


Figure 1.9

The bias current of an FET op amp is the leakage current of the gate diffusion (or the leakage of the gate protection diode, which has very similar characteristics, in the case of a MOSFET). Such leakage currents double with every $10^{\circ}C$ increase in chip temperature so

that the bias current of an FET op amp is ONE THOUSAND TIMES GREATER at $125^{\circ}C$ than at $25^{\circ}C$. Obviously this can be important when choosing between a bipolar or FET input op amp, especially in high temperature applications.

In speaking of FET op amps, we have spoken generally of all kinds of FETs, both junction (JFETs) and MOS (MOSFETs). In practice, op amps using bipolar technology and JFETs (BiFET and similar technologies) have far better performance than op amps using MOSFET or CMOS technology. One or two manufacturers do make very high performance op amps with MOS or CMOS input stages, but in general, MOS and CMOS op amps have poor offset and drift, poor voltage noise, and poor high-frequency performance, and even their power consumption is barely

lower than that of bipolar op amps with comparable, or even better, performance. (CMOS is a low-power process when used for logic because it does not pass current except when switching, but an op amp requires a standing or quiescent current, therefore a CMOS op amp is not intrinsically low power.)

JFETs require more headroom than BJTs and are more difficult to operate at very low power supply voltages, since their pinchoff voltage is typically greater than a BJT's base-emitter voltage.

JFET VERSUS MOS / CMOS OP AMPS

- MOS and CMOS are not very good linear processes (with a few exceptions).
- They have poor offset voltage, drift, voltage noise and output drive, but Input Bias Current is very low.
- Although they can be low power, better performance at similar power can often be achieved with bipolar processes.

Figure 1.10

Chopper Stabilized Op Amps

The best bipolar op amps may have guaranteed offsets as low as $10\mu\text{V}$. If offsets lower than this are required, a different op amp topology is necessary. This is "chopper stabilization" - the input signal is converted to AC by modulation, amplified, and demodulated. Any offsets in the system are eliminated in the modulation/demodulation process.

Early chopper stabilized amplifiers actually used relays to chop the signal, but today such amplifiers are mono-

lithic and use MOS switches to do the job. Early monolithic amplifiers of this type had high noise at the chopping frequency (which may be between a few hundred Hz and a few tens of kHz). This high-frequency noise is less of a problem in the latest devices, which may contain quite effective filters at the chopper frequency (although careful layout and supply decoupling is still important with these parts), but switching noise is still the major problem with chopper stabilized op amps.

CHOPPER STABILIZED OP AMPS

- Use fairly fast switches to convert inputs into AC which is amplified and then demodulated
- Negligible DC errors result (zero offset voltage)
- Very noisy because of chopping action, therefore output must be heavily filtered or averaged
- Low Offset almost impossible to realize except at frequencies $< 0.1\text{Hz}$

Figure 1.11

Because of the technology used to manufacture them (frequently CMOS), many chopper-stabilized op amps have a voltage noise of several μV in the band 0.1-10 Hz, and it is therefore necessary to integrate their output for several seconds or tens of seconds if we wish to obtain the low offset of the which they are potentially capable. Not all systems allow such long integration times, and so a compromise becomes

necessary between offset and speed. For many applications, a bipolar op amp such as the OP-177, which has $10\mu\text{V}$ offset and low voltage noise, may be more practical. There is no doubt, however, that in applications where long integration times are acceptable, a chopper-stabilized op amp has virtually zero offset, less bias current than a bipolar op amp, and is the device of choice.

PRECISION OP AMP VERSUS CHOPPER: A COMPARISON OF CRITICAL PARAMETERS

	BIPOLAR	CHOPPER
OFFSET VOLTAGE	10-50 μV	<5 μV
OFFSET DRIFT	0.1 $\mu\text{V}/^\circ\text{C}$	~0 μV
OPEN LOOP GAIN	10 Million	10 Million
NOISE: HF GLITCH	None	>100mVp-p
NOISE: 0.1-10Hz	<0.2 $\mu\text{Vp-p}$	>1 $\mu\text{Vp-p}$
COST	Lower	Higher
EXTERNAL COMPONENTS	None	Some Require 2 Caps.
SATURATION RECOVERY	10-20 μs	>100ms to seconds

Figure 1.12

Rail-Rail Input Stages

With increasing emphasis on low voltage and single-supply operation, there is a demand for op amps whose input common-mode range includes both supply rails. Such a feature is undoubtedly useful in some applications, but engineers should recognize that there are relatively few applications where it is absolutely essential. These should be carefully distinguished from the many applications where common-mode range *close* to the supplies is necessary, but rail-rail is not.

The problem is that a true rail-rail input stage requires two long-tailed

pairs (see Figure 1.14), one of NPN BJTs (or N-channel FETs), the other of PNP (or P-channel devices). These two pairs have different offsets and bias currents, so that as the common-mode voltage changes so does V_{OS} and I_b . This results in relatively poor CMRR and common-mode Z_{in} . These specifications should be considered carefully when choosing a rail-rail input op amp for a non-inverting configuration. V_{OS} , I_b , and even CMRR may be quite good over part of the common-mode range and much worse in the region where operation shifts between the NPN and PNP devices.

RAIL-TO-RAIL INPUT STAGES

- Require two long-tailed pairs with inputs in parallel:
 One with NPN BJTs (or P-Channel FETs)
 One with PNP BJTs (or N-Channel FETs)
 - V_{OS} , I_b , and CMRR varies over their common mode range
- OR
- An on-chip inverter may be used to generate a power rail outside the external power supplies, but this adds noise.
 - It is often possible to use an op amp which allows the input signal to go to only *one* of the rails (usually ground)

Figure 1.13

OP-291 RAIL-TO-RAIL BIPOLAR INPUT STAGE

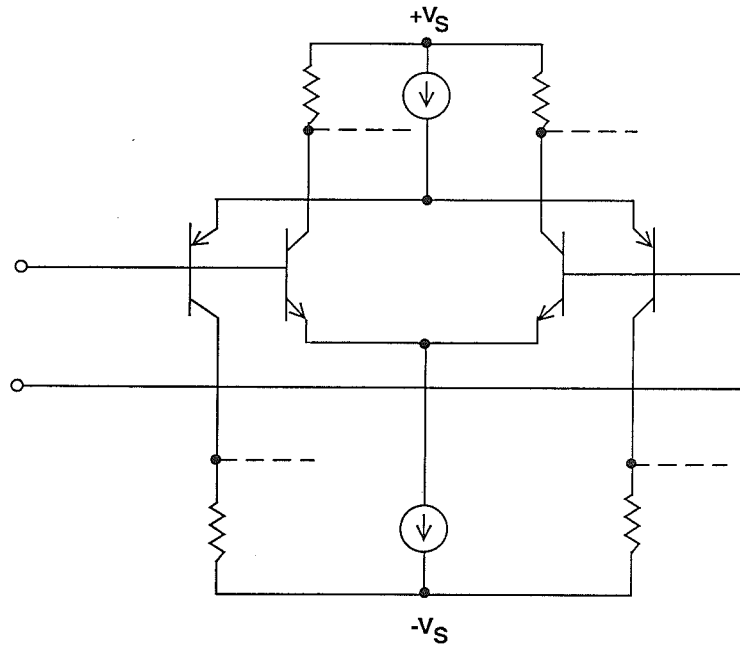


Figure 1.14

It is possible to make a monolithic op amp with a true rail-rail input using only NPN (or only PNP) transistors (or the corresponding FETs). This requires a small inverter on the chip to produce a power rail *outside* the external power supplies. Amplifiers of this type are not common, but do have good CMRR, and stable V_{OS} . Their problem is inverter noise — like chopper amplifiers they have an internal oscillator, and its signal tends to leak, even with careful decoupling.

In general, applications which appear to require true rail-rail inputs should be carefully evaluated to see if other techniques are possible. If they are not,

the amplifier should be chosen very carefully to ensure that its V_{OS} , I_b , CMRR and noise (voltage and current) are suitable for the application involved.

In many single-supply applications, it is required that the input go to only *one* of the supply rails (usually ground). Amplifiers which will handle zero-volt inputs are relatively easily designed using either PNP transistors (see OP-90 in Figure 1.15) or N-channel JFETs (see AD820 in Figure 1.16). P-channel JFETs can be used where inputs must include the positive supply rail (but not the negative rail) as shown in Figure 1.16 for the OP-282/OP-482.

OP-90 PNP INPUT STAGE ALLOWS INPUT TO GO TO THE NEGATIVE RAIL

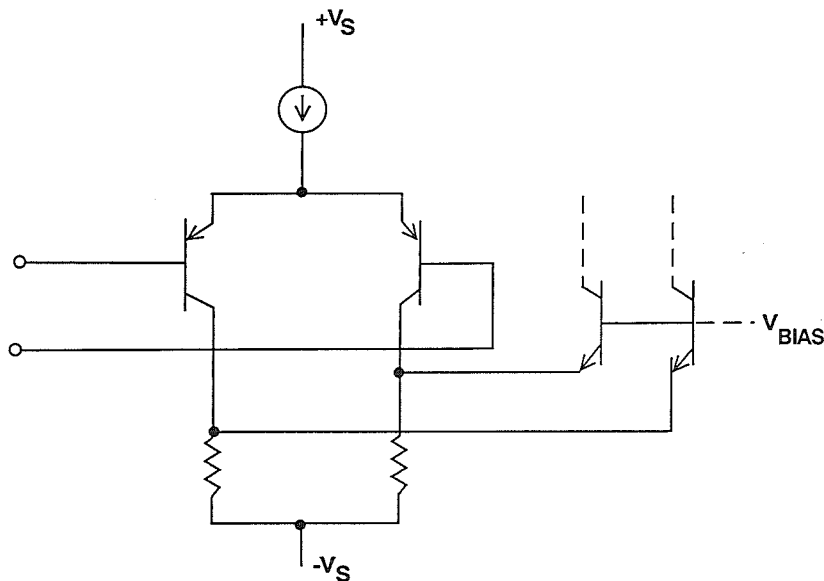


Figure 1.15

AD820/AD822 INPUT CAN INCLUDE NEGATIVE RAIL, OP-282/OP-482 CAN INCLUDE POSITIVE RAIL

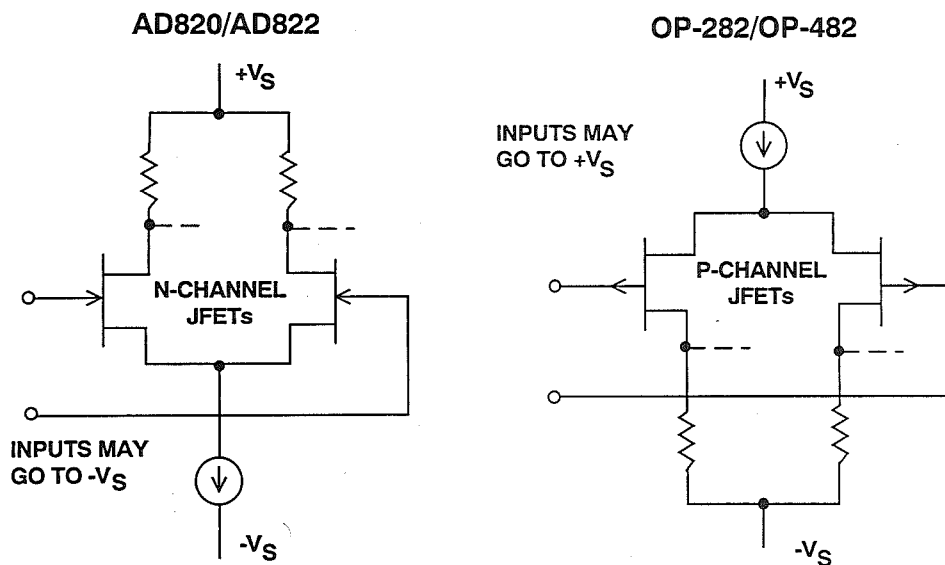


Figure 1.16

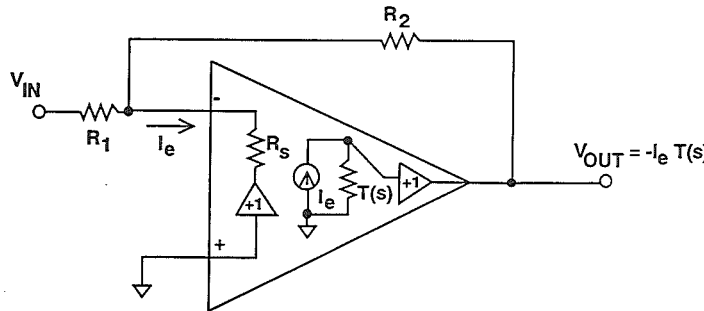
Transimpedance (Current-Feedback) Op Amps

A new type of high-frequency op amp has recently become popular: the *transimpedance* or *current feedback* op amp. We shall not discuss the reasons for its popularity in this section, other than to mention that under certain conditions, it has superior high frequency (HF) performance to the older (voltage feedback) architecture. (See Reference 3.)

The equivalent circuit for a current feedback amplifier is shown in Figure 1.17. Like the voltage feedback op amp, the current feedback type has inverting and non-inverting inputs. It differs from the voltage feedback op amp in that the two inputs are not identical in struc-

ture. The non-inverting input of a current feedback amplifier is a high impedance node, just as that of a voltage feedback op amp, but the inverting input is a low impedance, current input node. The signal at the non-inverting input is applied to the inverting input through a unity-gain buffer. Ideally, the inverting input is held at the same potential as the non-inverting and has zero input impedance. In practice, the input impedance R_s is of the order of a few tens of ohms, and there is an offset between the two inputs. This is comparable to the offset of a voltage feedback op amp, and may only be a few tens or hundreds of microvolts.

CURRENT FEEDBACK (TRANSIMPEDANCE) OP AMP EQUIVALENT CIRCUIT



$$\text{INVERTING SIGNAL GAIN} = - \left(\frac{R_2}{R_1} \right) \left(\frac{1}{1 + \frac{1}{LG}} \right) \quad \text{NON-INVERTING SIGNAL GAIN} = \left(1 + \frac{R_2}{R_1} \right) \left(\frac{1}{1 + \frac{1}{LG}} \right)$$

$T(s)$ = OPEN LOOP TRANSIMPEDANCE GAIN

$$\beta_{cf} = \text{FEEDBACK FACTOR} = \frac{R_s \parallel R_1}{R_s \parallel R_1 + R_2}$$

$$A_{cf}(s) = \text{OPEN LOOP VOLTAGE GAIN} = \frac{T(s)}{R_s}$$

$$\text{LOOP GAIN} = LG = A_{cf}(s) \beta_{cf} = \frac{T(s) \{ R_s \parallel R_1 \}}{R_s \{ R_s \parallel R_1 + R_2 \}}$$

Figure 1.17

The current entering the inverting input is multiplied by the *transimpedance open loop gain*, $T(s)$, to yield the output voltage. The *feedback factor* of the current feedback amplifier is different from the voltage feedback amplifier because of the low inverting input impedance, R_S . Solving the feedback equation yields the transfer function shown in Figure 1.17. Although the

expression for the current feedback amplifier loop gain is different from a voltage feedback amplifier, it can be used in exactly the same manner in determining the accuracy of the amplifier closed loop gain at any specific frequency. Figure 1.18 shows a simplified schematic of the AD846, a typical current feedback op amp.

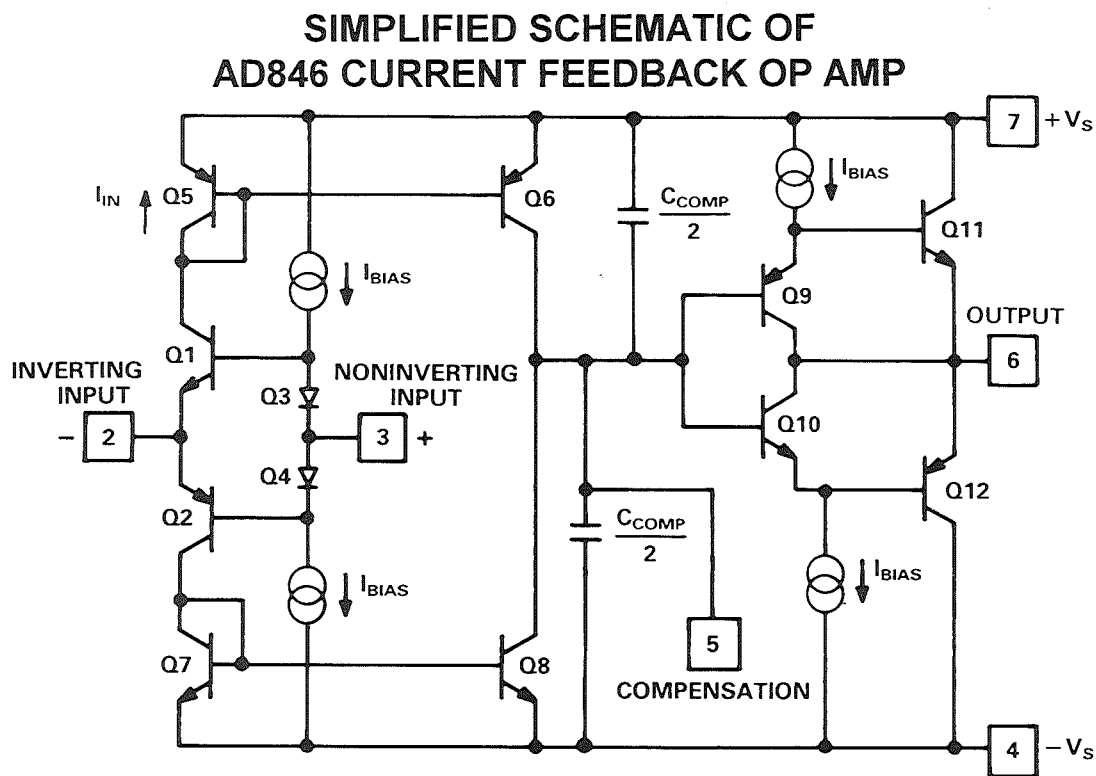


Figure 1.18

Comparison Between Voltage Feedback and Current Feedback Op Amps

The inverting mode transfer functions for the voltage feedback amplifier and the current feedback amplifier are compared in Figure 1.19. Notice that for the voltage feedback amplifier, the frequency-dependent term, $1/A(s)$, is multiplied by the noise gain of the

circuit, $(1 + R_2/R_1)$. This implies that the closed loop bandwidth is inversely proportional to the noise gain; hence, the product of the noise gain and the closed loop bandwidth is constant, i.e. there is a constant gain-bandwidth product.

COMPARISON OF VOLTAGE FEEDBACK AND CURRENT FEEDBACK INVERTER CLOSED LOOP GAIN EQUATIONS

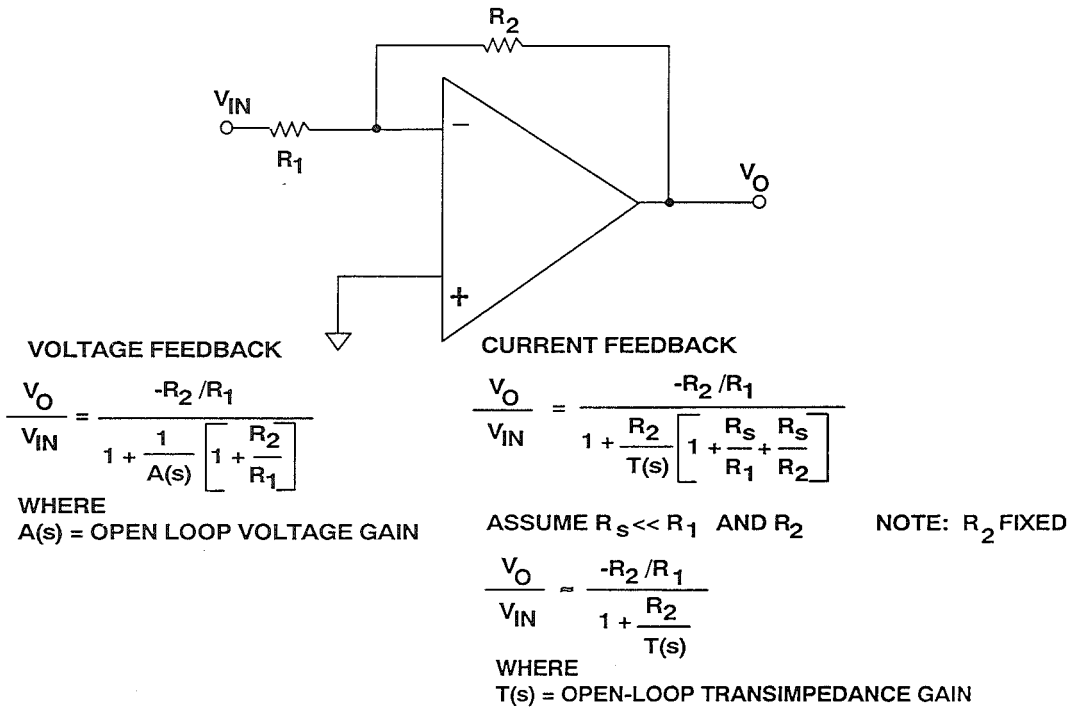


Figure 1.19

However, in the current feedback amplifier, if $R_s \ll R_1$ and R_2 , the closed loop bandwidth is relatively independent of the gain (R_2/R_1) and depends only upon the feedback resistor, R_2 . Furthermore, most current feedback amplifiers are optimized for maximum bandwidth with a particular value of R_2 . This implies that the closed loop bandwidth of a current feedback amplifier will remain fairly constant regardless of closed loop gain, provided the gain is changed by varying only R_1 . (Therefore, it is inappropriate to refer to the gain-bandwidth product of this type of amplifier). Increasing the feedback resistor, R_2 , lowers the bandwidth proportionally, while decreasing the value may lead to instability.

The requirement of a fixed, low-value (typically 400Ω to 1000Ω) feedback resistor becomes a significant disadvantage when using a current feedback op

amp in the inverting mode at large gains. For example, with the AD9617 optimum feedback resistor R_2 of 400Ω, the feedforward resistor R_1 must be 40Ω to achieve an inverting gain of 10. Driving the low value feedforward resistor may become a significant problem. Therefore, the non-inverting configuration is generally preferable when using current feedback amplifiers at high gains.

There are several important consequences of this new structure: (1) the device does not have a “gain-bandwidth product”; (2) bias currents are comparatively large, unmatched, may flow in either direction (like a bias-compensated op amp, and for the same reason: the external bias current is the *difference* of two larger internal currents), and may vary differently with temperature; and (3) while the voltage noise may be low, the current noise at

the two inputs is quite high. Additionally, the two noise currents are neither equal nor correlated, and neither do they necessarily have the same $1/f$ corner frequency.

These comments should not be interpreted as a condemnation of current feedback op amps, merely a warning that different considerations apply to their use than to the use of the classical voltage feedback amplifier. When properly used, they may offer wider

bandwidth, lower distortion, and lower voltage noise than a classical voltage feedback op amp. However, they are unstable with capacitive loads and capacitive feedback and may not be used in most classical active filter circuits. There is rarely any need to use current feedback amplifiers in DC or low frequency (LF) designs except perhaps as the output driver in a low noise, low distortion composite amplifier designed specifically for high current drive (Reference 2).

SUMMARY OF VOLTAGE FEEDBACK OP AMP CHARACTERISTICS

- **Symmetrical Inputs**
- **Equalization of Source Resistances Generally Reduces Effects of Input Bias Currents (except where bias current cancellation techniques are used)**
- **Largest Noise Source may be Input Voltage Noise or Input Current Noise depending on Impedance Levels**
- **Flexible Feedback Networks Allow Many Tradeoffs**
- **Constant Gain-Bandwidth Product**
- **May be Used as Integrators in Active Filters**

Figure 1.20

SUMMARY OF CURRENT FEEDBACK OP AMPS CHARACTERISTICS

- Non-Symmetrical Inputs (High Impedance Noninverting Input, Low Impedance Inverting Input)
- Input Bias Current Cancellation Schemes Don't Work because currents are poorly matched.
- Inverting Input Current Noise Usually Dominates
- Feedback Resistor Value Fixed for Optimum Performance
- Difficult to Use as Integrators (Oscillates with capacitive feedback)
- Bandwidth Remains Relatively Constant for Different Gains, therefore *Gain-Bandwidth Product* concept is meaningless
- Stray Capacitance on Inputs and Outputs will cause Peaking
- Offer no Advantage at DC or Low Frequencies

Figure 1.21

EFFECTS OF OVERDRIVE ON OP AMP INPUTS

There are several important points to be considered about the effects of overdrive on op amp inputs. The first is, obviously, damage. The data sheet of an op amp will give "absolute maximum" input ratings for the device. These may be expressed in terms of the supply voltage, or may not, but, unless the data sheet expressly says otherwise, maximum ratings apply only when supplies are present, and inputs should be held near zero in the absence of supplies.

A common type of rating expresses input voltage in terms of the supply, $V_{SS} \pm 0.3V$. In effect, neither input may go more than 0.3V outside the supply rails, whether they are on or off. If current is limited to 5mA or less, it

generally does not matter if inputs do go outside $\pm 0.3V$ *when the supply is off* (provided that no base-emitter reverse breakdown occurs). Problems may arise if the input is outside this range when the supplies are turned on - this can turn on parasitic SCRs in the device structure and destroy it within microseconds. This condition is called *latch-up*, and is much more common in digital CMOS than in linear processes used for op amps. If a device is known to be sensitive to latch-up, avoid the possibility of signals appearing before supplies are established. (When signals come from other circuitry using the same supply there is rarely, if ever, a problem.) Fortunately, most IC op amps are relatively insensitive to latch-up.

INPUT STAGE OVERVOLTAGE

- INPUT SHOULD NOT EXCEED ABSOLUTE MAXIMUM RATINGS (Usually Specified With Respect to Supply Voltages)
- A Common Specification Requires the Input Signal $< V_S \pm 0.3V$
- Input Voltage Should be Held Near Zero in the Absence of Supplies
- Input Stage Conduction Current Needs to be Limited (Rule of Thumb: 5mA)
- Avoid Reverse Bias Junction Breakdown in Input Stage Base-Emitter Junctions
- Differential and Common-Mode Ratings may Differ
- No Two Amplifiers are exactly the Same
- Some Op Amps Contain Input Protection (Voltage Clamps, Current Limits, or Both), but Absolute Maximum Ratings Must Still be Observed

Figure 1.22

A SCHOTTKY DIODE CLAMP KEEPS THE INPUT (ALMOST) WITHIN THE SUPPLIES, AND A RESISTOR LIMITS INPUT CURRENT

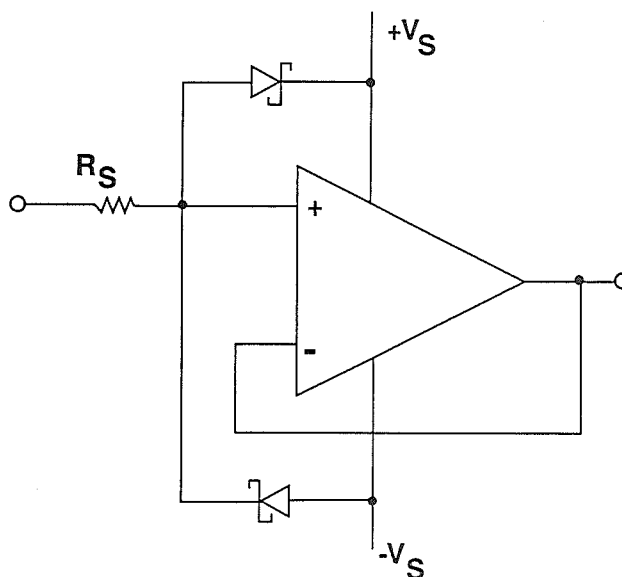


Figure 1.23

A common method of keeping the signal within the supplies is to clamp the signal to the supplies with schottky diodes as shown in Figure 1.23. This does not, in fact, limit the signal to $\pm 0.3V$ at all temperatures, but if the schottky diodes are at the same temperature as the op amp, they will limit the voltage to a safe level, even if they do not limit it at all times to within the data sheet rating. This is easily accomplished if over-voltage is only possible at turn-on, and diodes and op amp will always be at the same temperature then. If the op amp may still be warm when it is repowered, however, steps must be taken to ensure that diodes and op amp are at the same temperature when this occurs.

Many op amps have limited common mode or differential input voltage ratings. Limits on common-mode are usually due to complex structures in very fast op amps and vary from device to device. Limits on differential input avoid a damaging reverse breakdown of the input transistors (especially super-beta transistors). This damage can occur even at very low current levels. Limits on differential inputs may

also be needed to prevent internal protective circuitry from over-heating at high current levels when it is conducting to prevent breakdowns - in this case, a few hundred microseconds of over-voltage may do no harm. One should never exceed any "absolute maximum" rating, but engineers understand the reasons for the rating so that they can make realistic assessments of the risk of permanent damage should the unexpected occur.

If an op amp is over-driven *within* its ratings, no permanent damage should occur, but some of the internal stages may saturate. Recovery from saturation is generally slow, except for certain "clamped" op amps specifically designed for fast over-drive recovery. Over-driven amplifiers may therefore be unexpectedly slow.

Because of this reduction in speed with saturation (and also output stages unsuited to driving logic), it is generally unwise to use an op amp as a comparator. Nevertheless, there are sometimes reasons why op amps may be used as comparators. The subject is discussed in Reference 3.

INPUT STAGE OVERDRIVE

- Overdriving Op Amps (Within Absolute Maximum Ratings) does no Damage but may cause Saturation
- Saturation Recovery Times may be Long
- It is therefore Inadvisable to use Op Amps as Comparators (In General -- There may be Exceptions)

Figure 1.24

OP AMP OUTPUT STAGES

The earliest IC op amp output stages were NPN emitter followers with emitter current sources or resistive pull-downs (see Figure 1.25). Naturally they were far faster with positive-going signals than with negative ones. While all modern op amps have push-pull output stages of some sort, many are still, to a greater or lesser degree, asymmetrical and have a greater slew rate in one direction than the other. This asymmetry, which generally results from the use of IC processes with better NPN than PNP transistors, may also result in an ability to approach one supply more closely than the other in terms of output voltage swing.

If a process can make relatively well-matched PNP and NPN transistors,

then its output limiting levels and slew rates will be reasonably well matched. However, an output stage using BJTs cannot swing completely to its rails, but only to within the transistor saturation voltage of the rails (see Figure 1.26). For small amounts of load current (less than $100\mu\text{A}$), the saturation voltage may be as low as 5 to 10mV. For load currents of 10mA, the saturation voltage can increase to several hundred mV.

An output stage constructed of CMOS FETs can provide true rail-to-rail performance, but only under no-load conditions. If the output must source or sink current, the output swing is reduced by the voltage dropped across the FETs "on" resistance (typically 100Ω).

OP AMP OUTPUT STAGES USING
COMPLEMENTARY DEVICES ALLOW PUSH-PULL DRIVE

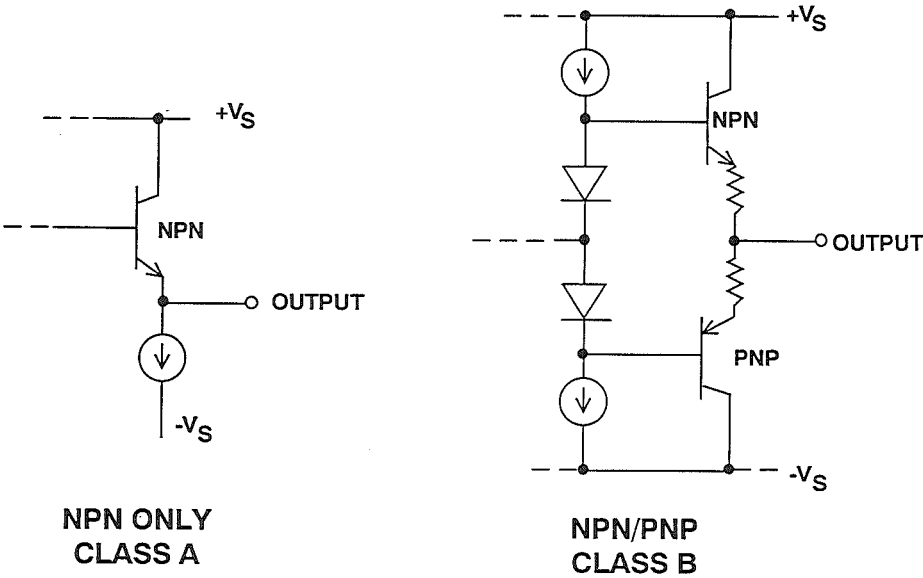


Figure 1.25

RAIL-TO-RAIL OUTPUT STAGES

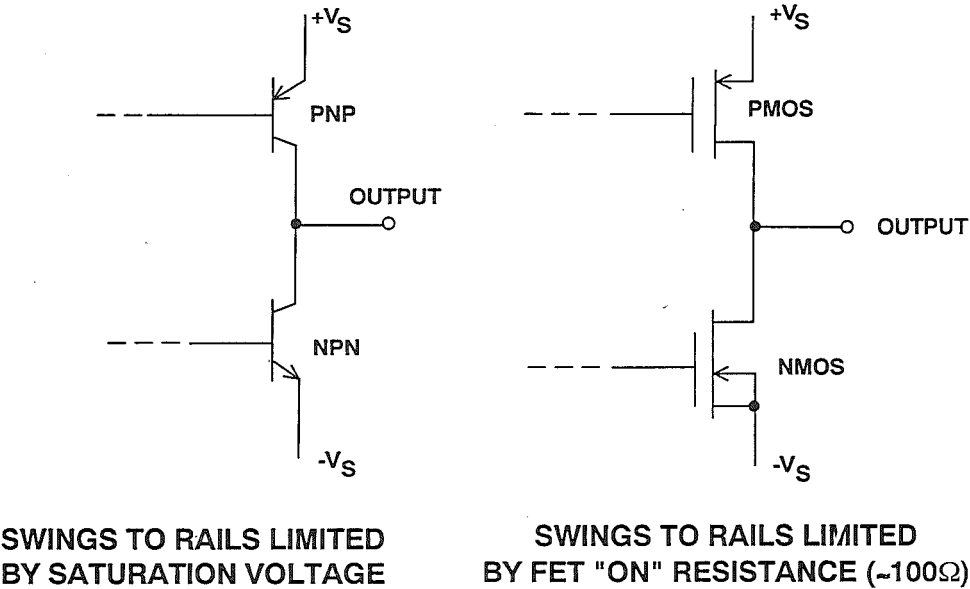


Figure 1.26

In many applications, it is only required that the output swing to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high

enough or is also grounded to that rail), but only slowly. An FET current source can replace the resistor and speed things up, but at a cost of increased complexity. CMOS and bipolar stages which will operate at the negative rail are shown in Figure 1.27.

OUTPUT STAGES WHICH ALLOW "NEGATIVE RAIL ONLY" OPERATION ARE OFTEN SUFFICIENT

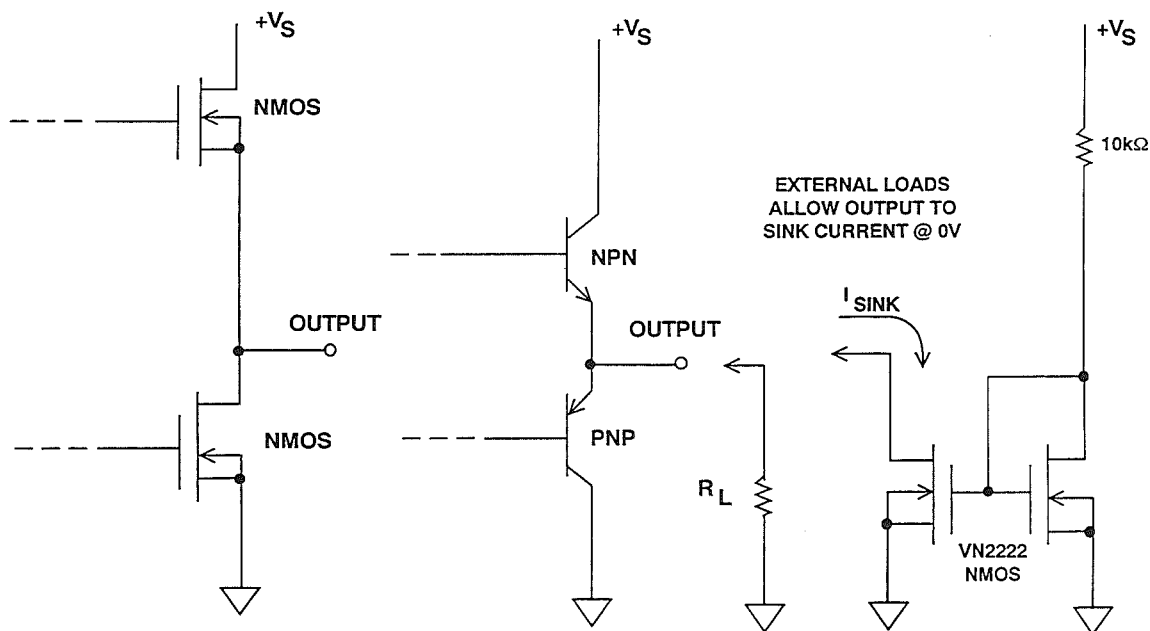


Figure 1.27

Low speed op amps generally have output stages which are protected against short circuits to ground or to either supply. Their output current is limited to a little more than 10mA. This has the additional advantage that it minimizes self-heating of the chip, and thus DC errors due to chip temperature differentials.

If an op amp is required with high precision and a large output current, it is advisable to use a separate output stage (within the loop) to minimize self-heating of the precision op amp. A simple medium power audio amplifier is often suitable. (There is an instrumen-

tation amplifier, not made by Analog Devices, which has a V_{OS} of $50\mu V$ and an I_{out} of 50mA — but you can't have both at the same time!)

High speed op amps cannot have output currents limited to such a low value, since it would affect their slew rate and ability to drive low impedances. Most high speed op amps will source and sink between 50-100mA, and few are limited to less than 30mA. Although many high speed op amps have short circuit protection, junction temperatures may be exceeded (because of the high short circuit current) resulting in device damage for prolonged shorts.

OP AMP OUTPUT STAGE PROTECTION

- Low Frequency op amps are generally protected against shorts to ground or either supply by a current limit of 10mA or greater.
- Op amps with high current outputs (including high speed op amps where current is needed to achieve high slew rate) are usually protected, but prolonged shorts may cause damage due to excessive junction temperatures.
- When high current *and* high precision are required, use a composite configuration with a precision op amp followed by a high current op amp (within the feedback loop). This avoids loss of accuracy due to non-uniform heating of the precision op amp chip.

Figure 1.28

OP AMP SPECIFICATIONS

Although voltage feedback and current feedback op amps have similar error terms and specifications, the application of each part warrants discussing some

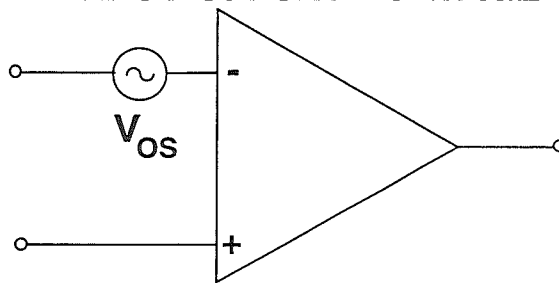
of the specifications separately. In the discussions to follow, this will be done where significant differences exist.

Input Offset Voltage

Ideally, if both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the “offset voltage”, V_{OS} . Input offset voltage is

modeled as a voltage source, $V_{OS,in}$ series with the inverting input terminal of the op amp as shown in Figure 1.29. The corresponding output offset voltage (due to V_{OS}) is obtained by multiplying the input offset voltage by the DC noise gain of the circuit $(1 + R_2/R_1)$.

INPUT OFFSET VOLTAGE



- **Offset Voltage:** The differential voltage which must be applied to the input of an op amp to produce zero output.
- **Ranges:**
 - ◆ Chopper Stabilized Op Amps: $< 1\mu V$
 - ◆ General Purpose Precision Op Amps: $50 - 500\mu V$
 - ◆ Best Bipolar Op Amps: $10-25\mu V$
 - ◆ Best FET Op Amps: $50-1000\mu V$
 - ◆ High Speed Op Amps: $100-2000\mu V$

Figure 1.29

Chopper stabilized op amps have a V_{OS} which is less than $1\mu V$ (but, as mentioned above, are difficult to use because of noise). The best bipolar op amps (super-beta or bias stabilized) can have offsets as low as $10\mu V$, and the best FET types have about $50\mu V$. Generally, "precision" op amps will have $V_{OS} < 0.5mV$, although some high speed ones may be a little worse than this.

Input offset voltage is often measured by measuring the op amp's output offset voltage and dividing by the noise gain of the circuit (see Figure 1.30). This method will yield accurate results if the effects of input bias current on the total output offset voltage are negligible.

FET input op amps have low bias currents at room temperature, so this method works satisfactorily. In the case of significant bias currents where I_{b+} and I_{b-} are not equal (as in the case of current feedback op amps), an instrumentation amplifier connected to the op amp input terminals (through isolation resistors) should be used to provide the gain for the measurement (right-hand diagram in Figure 1.30). The offset voltage of the instrumentation amp (measured with S closed) must then be subtracted from the final measurement. Another circuit for measuring input offset voltage (independent of bias currents) is shown in Figure 1.36.

MEASURING INPUT OFFSET VOLTAGE

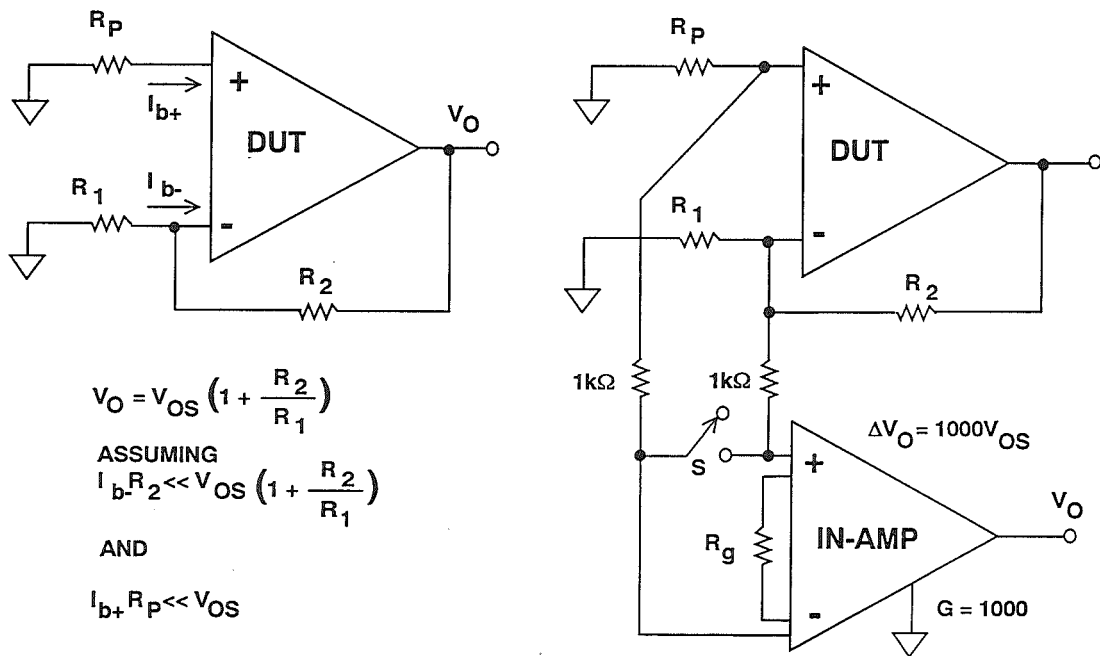


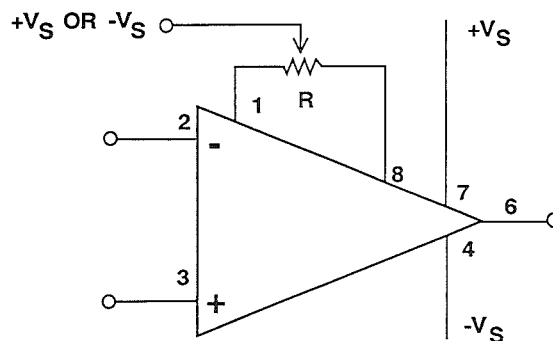
Figure 1.30

Offset Adjustment

Many op amps have pins available for optional offset null. Generally, two pins are joined by a potentiometer, and the wiper goes to one of the supplies as shown in Figure 1.31. If the wiper is accidentally connected to the wrong supply, the op amp will probably be destroyed — this is a common problem when one type of op amp is replaced with another. The range of offset adjustment in a well-designed op amp is

no more than two or three times the maximum V_{OS} of the lowest grade device, in order to minimize the sensitivity of these pins. Nevertheless, the voltage gain of an op amp at its offset adjustment pins may actually be greater than the gain at its signal inputs! It is therefore very important to keep these pins free of noise. It is inadvisable to have long leads from an op amp to a remote potentiometer.

OFFSET ADJUSTMENT PINS



- Wiper connection may be to either $+V_S$ or $-V_S$ depending on op amp
- R value depends on op amp, $10\text{k}\Omega$ - $100\text{k}\Omega$ typical
- Use to null out input offset voltage, not system offsets!
- There may be high gain from offset pins to output -- Keep them quiet!
- Nulling offset causes increase in offset temperature coefficient, approximately $4\mu\text{V}/^\circ\text{C}$ for 1mV offset null for FET inputs

Figure 1.31

As was mentioned above, the offset drift of an op amp with temperature will vary with the setting of its offset adjustment. The internal adjustment terminals should therefore be used only to adjust the op amp's own offset, not to correct any system offset errors, since this would be at the expense of increased temperature drift. The drift penalty for a FET input op amp is in the order of $4\mu\text{V}/^\circ\text{C}$ for each millivolt of nulled offset voltage. It is generally better to control the offset voltage by proper selection of devices and device grades.

If an op amp does not have offset adjustment pins, and it is necessary to adjust the amplifier and system offsets, or if the offset adjustment is to be done with a DAC (which is not well-suited to interfacing with op amp offset adjustment pins), then offset correction may be performed in a number of ways.

Injecting current into the inverting input is the simplest method when using the op amp in the inverting mode (see Figure 1.32). The disadvantage of this method is that there is an increase in noise gain due to R_3 and the potentiometer resistance. The resulting increase in noise gain may be reduced by making V_R large enough so that R_3 can be made much greater than R_1 and R_2 .

The second circuit in Figure 1.32 shows how to create an output offset by injecting the offset current into the non-inverting input. This circuit results in no increase in noise gain, but requires the addition of R_p . If the op amp has matched input bias currents, then R_p should equal the parallel combination of R_1 and R_2 (for bias current cancellation). Otherwise, R_p should be less than 50Ω . It may be advisable to decouple R_p at HF.

INVERTING OP AMP LEVEL SHIFTERS

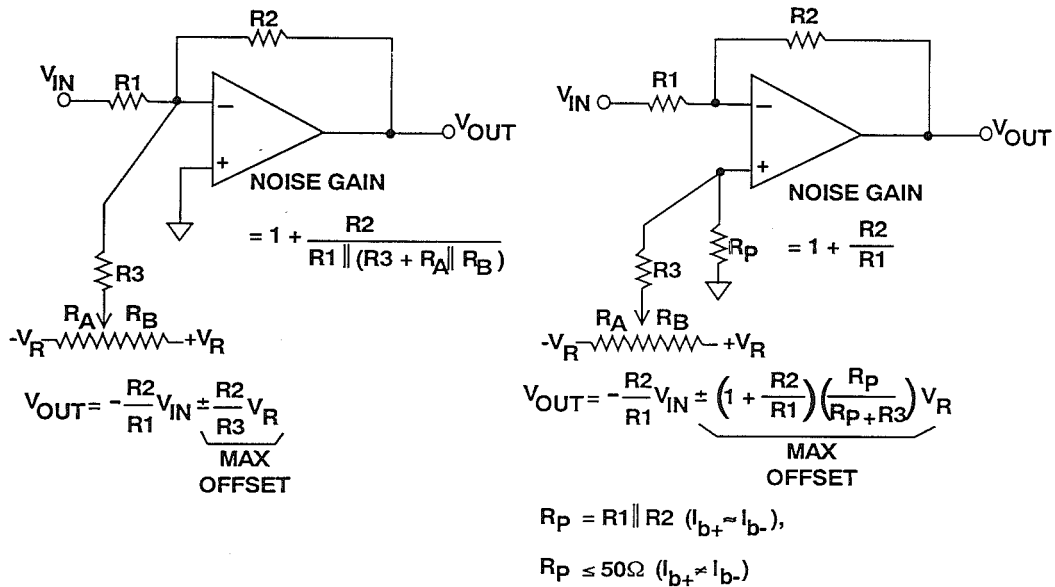


Figure 1.32

The circuit shown in Figure 1.33 can be used to level shift the output when using the op amp in the non-inverting mode. This circuit works well for small offsets where R3 can be made much greater than R1. Otherwise, the signal

gain will be affected as the offset potentiometer is adjusted. The gain may be stabilized, however, if R3 is connected to a fixed low impedance reference voltage source.

NON-INVERTING OP AMP LEVEL SHIFTER

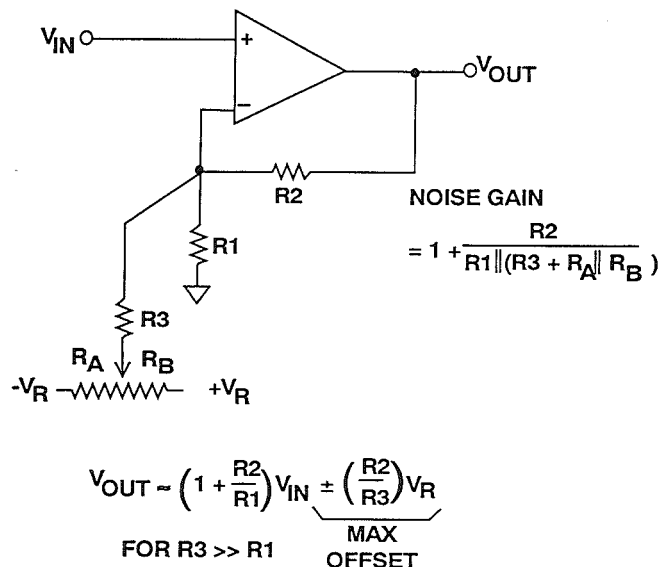


Figure 1.33

Input Offset Voltage Drift and Aging Effects

V_{OS} varies with temperature, and its temperature coefficient is known as TCV_{OS} . As we have mentioned, offset drift is affected by offset adjustments to the op amp, but when it has been minimized, it may be as low as $30\text{nV}/^{\circ}\text{C}$ (typical value for OP-177E). More typical values for a range of general purpose precision op amps lie in the range $1 - 10\mu\text{V}/^{\circ}\text{C}$.

Most op amps have a specified value of TCV_{OS} , but some, instead, have a second value of maximum V_{OS} which is

guaranteed over the operating temperature range. Such a specification is less useful, because there is no guarantee that TCV_{OS} is constant or monotonic.

V_{OS} changes as time passes. Aging is generally specified in $\mu\text{V}/\text{month}$ or $\mu\text{V}/1000\text{ hrs}$, but this is misleading. Since aging is a "drunkard's walk" phenomenon it is proportional to the *square root* of the elapsed time. An aging rate of $1\mu\text{V}/1000\text{ hr}$ becomes about $3\mu\text{V}/\text{yr}$, not $9\mu\text{V}/\text{yr}$.

INPUT OFFSET VOLTAGE DRIFT (TCV_{OS}) AND AGING

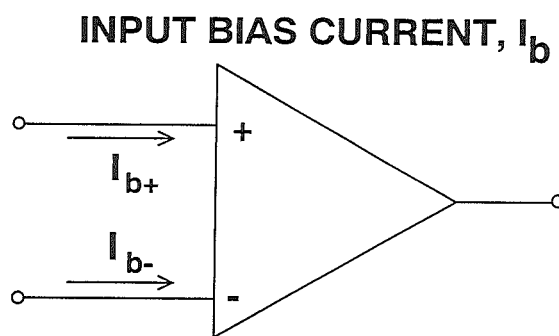
- Values may range from $30\text{nV}/^{\circ}\text{C}$ (typical for OP-177E) to $10\mu\text{V}/^{\circ}\text{C}$ or more
- Internal offset adjustments using null pins make drift worse
- Specification may be replaced by a specification of maximum V_{OS} over temperature -- this is less useful
- Aging in analog ICs is a "drunkard's walk" or "random walk" phenomenon, not linear. This means that the accumulated error is proportional to the *square root* of the elapsed time.
- $1\mu\text{V} / 1000\text{ hr} \approx 3\mu\text{V} / \text{year} \approx 9\mu\text{V} / 10\text{ year}$

Figure 1.34

Input Bias Current, I_b

Ideally, no current flows into the input terminals of a voltage feedback op amp. In practice there is always a bias current, I_b (see Figure 1.35). Values of I_b range from 60fA (about one electron every three microseconds) in the AD549 electrometer to tens of microamperes in some high speed op amps. Op amps with simple input structures using BJT

or FET long-tailed pair have bias currents which flow in one direction. More complex input structures (bias-compensated and transimpedance op amps) may have bias currents which are the difference between two or more internal current sources and may flow in either direction.



- A very variable parameter
- I_b can vary from 60 fA (1 electron every 3 μ s) to many μ A depending on the device.
- Some structures have well-matched I_b , others do not.
- Some structures' I_b varies little with temperature, but FET op amp's I_b doubles with every 10°C rise in temperature.
- Some structures have I_b which may flow in either direction.

Figure 1.35

Bias current is a problem to the op amp user because it flows in impedances and produces voltages, which add to system errors. Consider a non-inverting unity gain buffer driven from a source impedance of 1M Ω . If I_b is 10nA, it will introduce an additional 10mV of error into the system. If the designer forgets I_b and uses capacitive coupling, the circuit will not work at all. If I_b is low enough, it may work for a while while the capacitor charges, giving even more

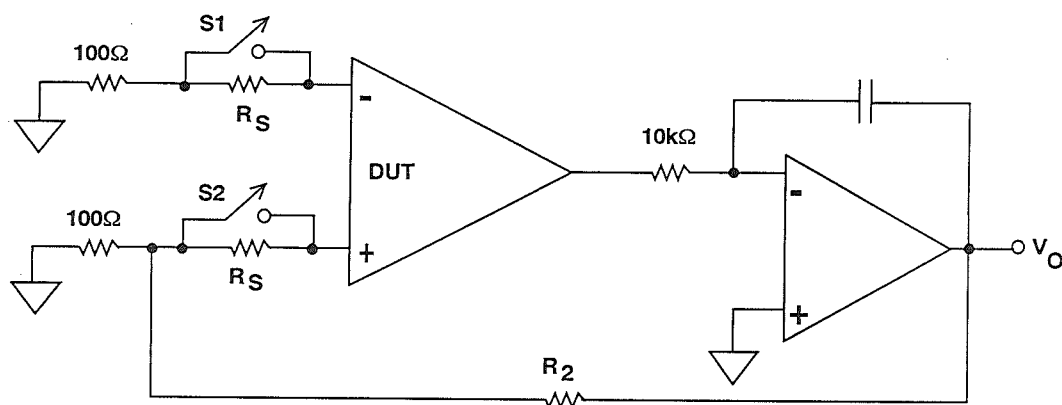
misleading results. If the capacitor is an electrolytic type, its leakage may be enough to pass the bias current - in some cases, so that we have a circuit which only works with *some* op amps and *some* capacitors.

Bias current (as well as input offset voltage) may be measured using the test circuit of Figure 1.36. A large resistance, R_s , is inserted in series with the input under test, creating an appar-

ent additional offset voltage equal to $I_b R_S$. If the actual V_{OS} has been measured and recorded, the change in apparent V_{OS} due to the change in R_S can be determined and I_b easily computed. The *offset current* may then be

calculated by taking the difference between the bias current on the inverting input and the bias current on the noninverting input. Typical R_S values vary from $100\text{k}\Omega$ for bipolar op amps to $1000\text{M}\Omega$ for some FET input devices.

MEASURING INPUT BIAS CURRENT



$R_S \gg 100\Omega$ ($100\text{k}\Omega$ TO $1\text{G}\Omega$)

S1 CLOSED TO TEST I_{b+}

S2 CLOSED TO TEST I_{b-}

BOTH CLOSED TO TEST V_{OS}

BOTH OPEN TO TEST I_{OS}

$$V_O = \left(1 + \frac{R_2}{100}\right) V_{OS} + \left(1 + \frac{R_2}{100}\right) I_{b+} R_S - \left(1 + \frac{R_2}{100}\right) I_{b-} R_S$$

Figure 1.36

Extremely low bias currents must be measured by integration techniques. The current is used to charge a capacitor, and the rate of change is measured. If the capacitor and general circuit leakage is negligible (this is very difficult to ensure when currents of under

10fA are to be measured), the current may be calculated directly from the rate of change of the output of the test circuit (see Figure 1.37) when the switch which short-circuits the appropriate capacitor is opened.

MEASURING LOW INPUT BIAS CURRENT

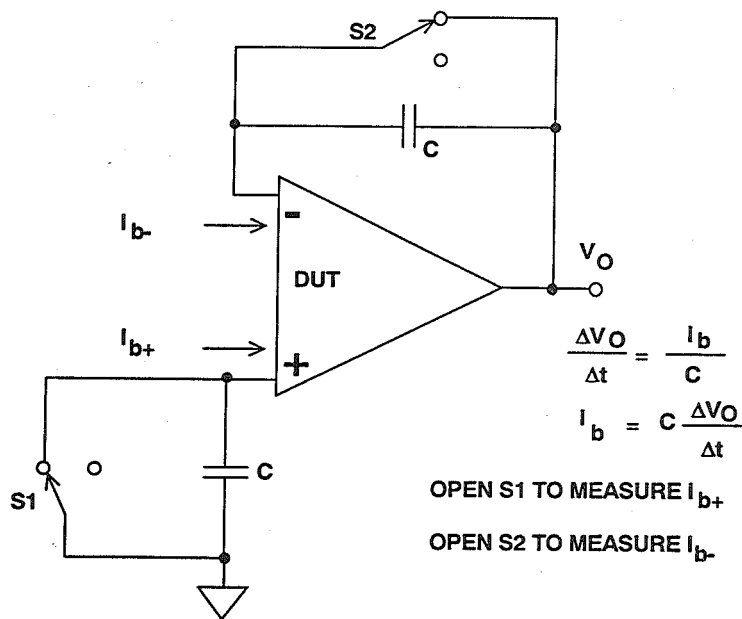


Figure 1.37

Bias Current Cancellation (External to the Op Amp)

If the bias currents of an op amp are approximately equal (which is the case with simple bipolar op amps, but not bias compensated ones), then a bias compensation resistor, R_3 , (where $R_3 = R_1 \parallel R_2$) will introduce a voltage drop in the non-inverting input to compensate the drop in the parallel

combination of R_1 and R_2 in the inverting input (see Figure 1.38). If R_3 is more than $1k\Omega$ or so, it should be decoupled with a capacitor to prevent HF instability. This form of bias cancellation is useless where bias currents are not well-matched, and will, in fact, make matters worse unless they are.

BIAS CURRENT CANCELLATION

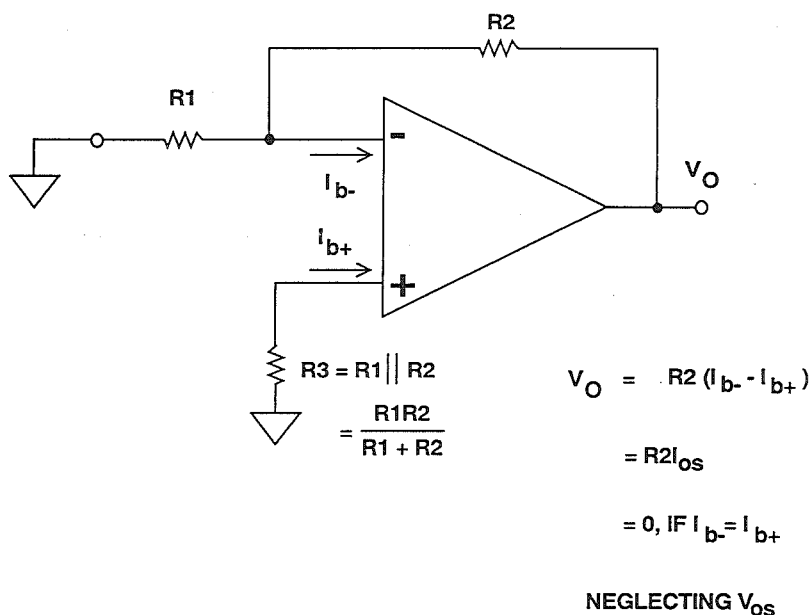


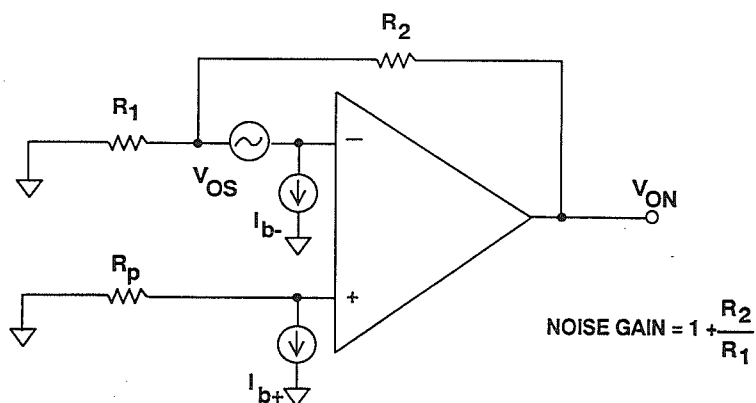
Figure 1.38

Calculation of Total Output Offset Error Due to I_b and V_{os}

The equations shown in Figure 1.39 are useful in reflecting all the offset and

bias current errors to the output of the op amp.

MODEL FOR CALCULATING TOTAL OP AMP OUTPUT VOLTAGE OFFSET



$$V_O = \pm V_{os} \left[1 + \frac{R_2}{R_1} \right] \pm I_{b+} R_p \left[1 + \frac{R_2}{R_1} \right] \pm I_{b-} R_2$$

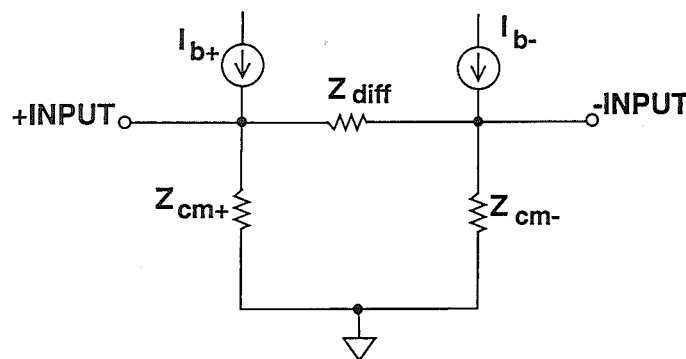
Figure 1.39

Input Impedance

Voltage feedback operational amplifiers normally have both differential and common-mode input impedance specified. Transimpedance (current feedback) op amps normally specify the impedance to ground at each input. Different models may be used for differ-

ent voltage feedback op amps, but in the absence of other information, it is usually safe to use the model in Figure 1.40. In this model the bias currents flow into the inputs from perfect (infinite impedance) current sources.

INPUT IMPEDANCE (VOLTAGE FEEDBACK)



- Z_{cm+} and Z_{cm-} are the common-mode input impedance. The figure on the data sheet is for one, not both, but they are approximately equal. Z_{diff} is the differential input impedance.
- They are high resistance ($10^5 - 10^{12}\Omega$) in parallel with a small shunt capacitance (sometimes as high as 25pF).
- In most practical circuits, Z_{cm-} is swamped by negative feedback.

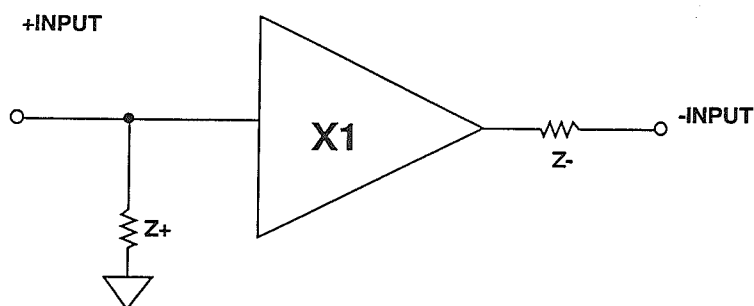
Figure 1.40

The common-mode input impedance specified on the data sheet (Z_{cm+} and Z_{cm-} in the diagram) is the impedance from either input to ground (NOT from both to ground). The differential input impedance (Z_{diff}) is the impedance between the two inputs. They are usually resistive and high ($10^5 - 10^{12}\Omega$) with some shunt capacitance (generally a few pF, sometimes as much as 20-25 pF). In most practical op amp circuits, the impedance at the inverting

input is reduced to a very low value by negative feedback and only Z_{cm+} and Z_{diff} are of any importance.

The model for a transimpedance (current feedback) op amp is even simpler and is shown in Figure 1.41. Z_+ is resistive, generally with some shunt capacitance, and high ($10^5 - 10^9\Omega$) while Z_- is reactive (L or C, depending on the device) but has a resistive component of 10 - 100 Ω , varying from type to type.

INPUT IMPEDANCE (CURRENT FEEDBACK)



- Z_+ is high resistance ($10^5 - 10^9 \Omega$) with little shunt capacitance.
- Z_- is low and may be reactive (L or C) The resistive component is $10 - 100 \Omega$

Figure 1.41

Open-Loop Gain

The open-loop voltage gain of most voltage feedback op amps is high. Values of 50,000 to 100,000,000 are common. Some fast op amps have lower open-loop gain, but gains of less than a few thousand are usually unsatisfactory for high accuracy applications. The open loop gain is not stable with temperature and can vary quite widely from device to device of the same type, so it is important that it be reasonably high.

Since a voltage feedback op amp has voltage in and voltage out, its open loop gain is a ratio and dimensionless, and no unit is therefore necessary. However,

data sheets sometimes express gain in V/mV instead of V/V for the convenience of using smaller numbers.

Current feedback op amps have a current input and a voltage output, so the open loop *transimpedance gain* is expressed in volts per ampere or ohms (or $k\Omega$ or $M\Omega$). Values usually lie between hundreds of $k\Omega$ and tens of $M\Omega$.

In many signal processing applications, AC specifications such as bandwidth, settling time, and distortion are more important than open-loop gain.

OPEN-LOOP GAIN

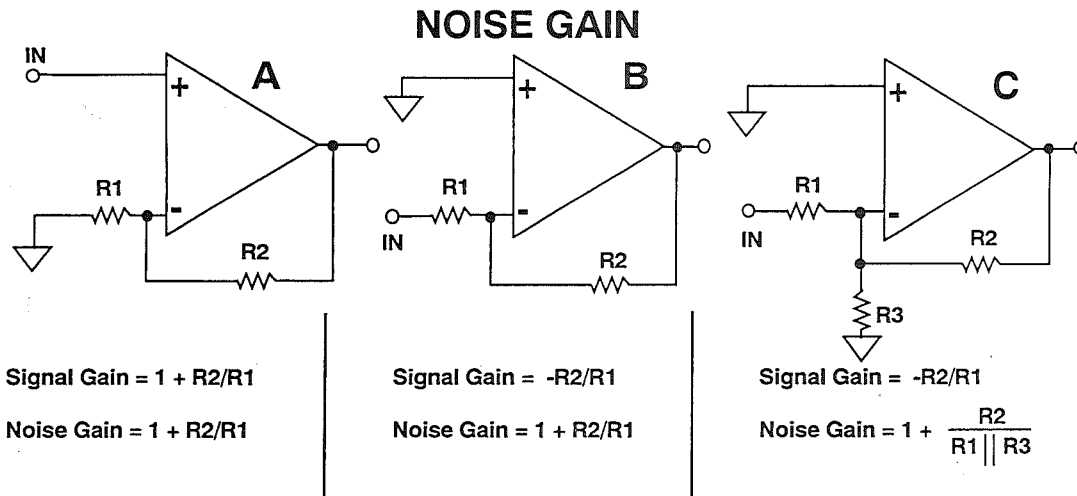
- Voltage Feedback Op Amps:
 - ◆ Volts Out / Volts In (Dimensionless)
 - ◆ Generally in the Range of 50,000 to 100,000,000 (94 to 160dB)
 - ◆ Sometimes Divided by 1,000 and expressed as Volts/millivolt.
- Transimpedance (Current Feedback) Op Amps:
 - ◆ Volts Out / Current In (Resistance)
 - ◆ Generally in the Range of 200k Ω to 50M Ω

Figure 1.42

Noise Gain

Consider an op amp and two resistors, R1 and R2, arranged as shown in Figure 1.43 (they need not be resistors, they could be complex impedances Z1 and Z2). If we ground R1 and apply a signal to the non-inverting input, we see a signal gain of $1 + R2/R1$ (left-hand diagram, Figure 1.43). If we ground the

non-inverting input and apply the signal to R1, we see a signal gain of $-R2/R1$ (center diagram, Figure 1.43). In both cases, the voltage noise of the op amp itself (as well as the input offset voltage) sees a gain of $1 + R2/R1$, which is known as the *noise gain* of the op amp.



- Voltage Noise and Offset Voltage of the op amp are reflected to the output by the Noise Gain.
- Noise Gain, not Signal Gain, is relevant in assessing stability.
- Circuit C has unchanged Signal Gain, but higher Noise Gain, thus better stability, worse noise, and higher output offset voltage.

Figure 1.43

The noise gain and the signal gain need not be equal, but it is the noise gain which is relevant in assessing stability. It is sometimes possible to alter the noise gain while leaving signal gain unaffected. Consider the inverting amplifier above: if we add a third resistor, $R3$, from the inverting input to

ground, the signal gain is unaffected, but the noise gain is increased to $1 + R2/(R1 || R3)$ (right-hand diagram, Figure 1.43). This provides a means of stabilizing an unstable inverting amplifier - at the cost of worse signal-to-noise ratio, less loop gain, and increased sensitivity to input offset voltage.

Closed-Loop Gain

Operational amplifiers are generally used in closed-loop applications where gain is determined by negative feedback. In the discussion of noise gain above, we assumed that the open loop gain was infinite, and the closed-loop gain was determined only by the resistor ratios. This is not actually the case.

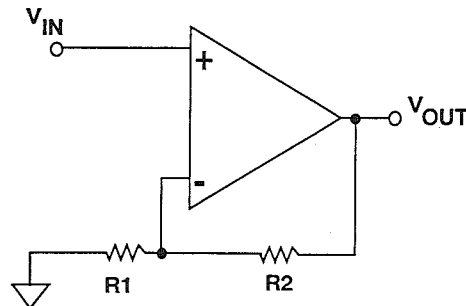
The expression for the gain of a closed-loop amplifier involves the open-loop gain. If G is the actual gain, N_G is the noise gain defined by the resistors R_1 and R_2 , and A is the open-loop gain of the amplifier, then

$$G = N_G - \frac{N_G^2}{N_G + A} = \frac{N_G}{\frac{N_G}{A} + 1}$$

Although this equation may be used to calculate low-frequency gain errors, it may also be used at higher frequencies, with R_1 and R_2 replaced by complex impedances Z_1 and Z_2 , and A by $A(s)$ (the gain at the frequency of interest) to determine actual HF gain.

The same equation is applicable to both voltage feedback and current feedback op amps. In the case of a current feedback op amp, however, A is obtained by dividing the open loop transimpedance gain T_z by the inverting input impedance R_s , i.e., $A = T_z/R_s$.

CLOSED-LOOP GAIN IS AFFECTED BY FINITE OPEN-LOOP GAIN



$$N_G = 1 + \frac{R_2}{R_1}$$

$$\blacksquare \frac{V_{OUT}}{V_{IN}} = G = N_G - \frac{N_G^2}{N_G + A} = \frac{N_G}{\frac{N_G}{A} + 1}$$

■ A = Open Loop Gain

■ For Current Feedback, $A = T/R_s$, where
 T = Open-Loop Transimpedance Gain
 R_s = Inverting Input Resistance

Figure 1.44

Op Amp Frequency Response - Introduction

There are a number of issues to consider when discussing the frequency response of op amps. Some are relevant to both voltage- and current feedback types, some apply to one or the other, but not to both. Issues which vary with type are usually related to small-signal performance, while large-signal issues mostly apply to both.

A good working definition of "large-signal" is where the frequency limit is set by the slew rate measured at the output stage, rather than the pole(s) of the small signal response. We shall therefore consider large signal parameters applying to both types of op amp before we consider those parameters where they differ.

OP AMP FREQUENCY RESPONSE

- Small-signal frequency response issues differ between voltage feedback and current feedback op amps
- Large signal issues are generally common to both
- The difference between small-signal and large-signal is that *slew rate* limits large-signal frequency response
- In general, the faster an op amp the more supply current it draws, and the more output current it may need to source

Figure 1.45

Frequency Response - Slew Rate and Full-Power Bandwidth

The slew rate of an amplifier is the maximum rate of change of voltage at its output. It is expressed in V/s (or, more probably, V/ μ s). We have mentioned earlier why op amps might have different slew rates during positive- and negative going transitions, but for this analysis we shall assume that good fast op amps have reasonably symmetrical slew rates.

If we consider a sine wave with a pk-pk amplitude of $2V_p$ and frequency f , the expression for the output voltage is:

$$v(t) = V_p \sin 2\pi f t \quad [1]$$

This has a maximum slew rate:

$$\left. \frac{dv}{dt} \right|_{\max} = 2\pi f V_p \quad [2]$$

We can thus see that the maximum frequency at which slew limiting *does not occur* is directly proportional to slew rate and inversely proportional to the amplitude of the signal. This allows us to define the "full-power bandwidth" (FPBW) of an op amp as the maximum frequency at which slew limiting does not occur at maximum output. This may be calculated by letting $2V_p$ in equation [2] equal the maximum pk-pk swing of the amplifier, dV/dt equal the slew rate, and solving for f :

$$\text{FPBW} = \text{Slew Rate} / 2\pi V_p \quad [3]$$

It is important to realize that both slew rate and full-power bandwidth can also depend somewhat on the power supply voltage being used and the load the amplifier is driving (particularly capacitive).

SLEW RATE AND FULL-POWER BANDWIDTH

■ Slew Rate = Maximum rate at which the output voltage of an op amp can change

■ Ranges: A few volts/ μ s to several thousand volts/ μ s

■ For a sinewave, $V_{\text{out}} = V_p \sin 2\pi f t$

$$dV/dt = 2\pi f V_p \cos 2\pi f t$$

$$(dV/dt)_{\max} = 2\pi f V_p$$

■ If V_p = full output span of op amp, then

$$\text{Slew Rate} = (dV/dt)_{\max} = 2\pi \cdot \text{FPBW} \cdot V_p$$

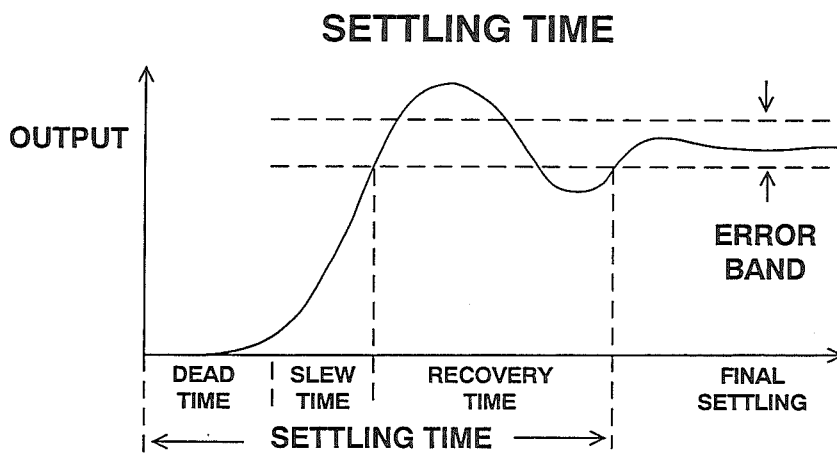
$$\text{FPBW} = \text{Slew Rate} / 2\pi V_p$$

Figure 1.46

Frequency Response - Settling Time

The settling time of an amplifier is defined as the time it takes the output to respond to a step change of input and come within *and remain within* a defined error band, as measured relative to the 50% point of the input pulse (see Figure 1.47). There is no natural error band for an op amp (a DAC naturally has an error band of 1 LSB, or perhaps $\pm 1\text{LSB}$), so one must be chosen and defined. What is chosen will depend on the performance of the op amp, but since the value chosen will vary from

device to device, comparisons are very difficult. This is true because settling is not linear, and many different time constants may be involved. Examples are early op amps using dielectrically isolated (DI) processes. These had very fast settling to 1% of full-scale, but they took almost forever to settle to 10-bits (0.1 %). Similarly, some very high precision op amps have thermal effects which cause settling to 0.001% or better to take tens of ms, although they will settle to 0.025% in a few μs .



- Error band is usually defined to be a percentage of the step 0.1%, 0.05%, 0.01%, etc.
- Settling time is non-linear; it may take 30 times as long to settle to 0.01% as to 0.1%.
- Manufacturers often choose an error band which makes the op amp look good.

Figure 1.47

Measuring fast settling time to high accuracy is difficult. Great care is required in order to generate fast, highly accurate, low noise, flat top pulses. Step voltages will overdrive most oscilloscope front ends when the input is set for high sensitivity. The test setup shown in Figure 1.48 is useful in making settling time measurements on op amps operating in the inverting

mode. The signal at the "false summing junction" represents the difference between the output and the input multiplied by the constant k , i.e. the ERROR signal. Schottky diode clamps help prevent scope overdrive and allows the use of high sensitivity. If $R_1=R_2$, then $k=0.5$. The error band at the ERROR output will be 5mV for 0.1% settling with a 10V input step.

MEASURING SETTLING TIME USING A "FALSE SUMMING NODE"

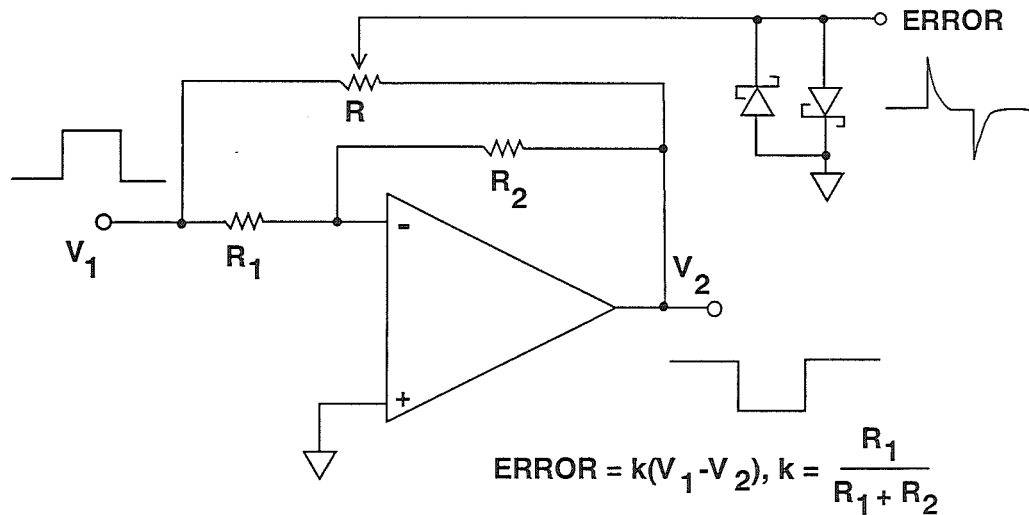


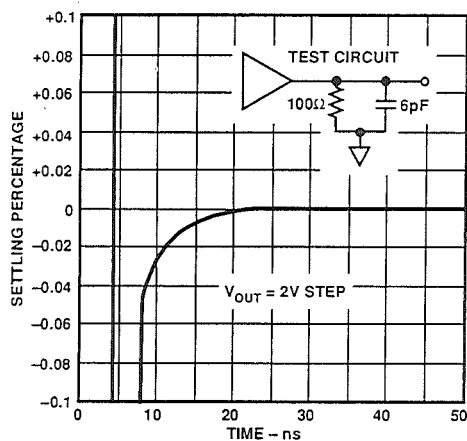
Figure 1.48

Certain digitizing scopes (such as the Data Precision Model 640 plug-in) can be used to measure the output waveform directly without overdrive. This allows measurements of settling time in both the inverting and non-inverting

modes. An example of the output step response to a flat pulse input for the AD9622 op amp is shown in Figure 1.49. Photos are shown for both short and long-term settling times.

MEASURING SETTLING TIME DIRECTLY USING A DIGITIZING PLUG-IN

SHORT TERM



LONG TERM

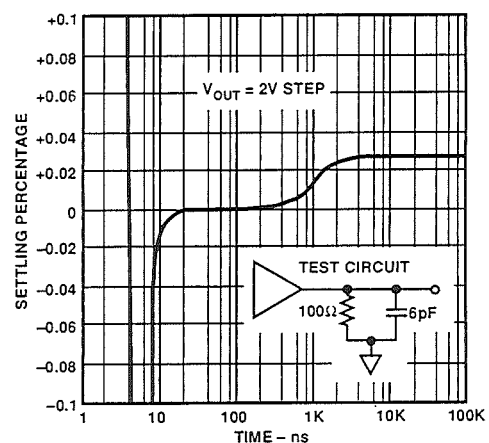


Figure 1.49

Frequency Response - Capacitive Loads

When an op amp drives a capacitive load, its output stage is slowed down. This puts an additional pole in the frequency response and, since op amps take negative feedback from their output stage, may cause instability and oscillation. (An example of the way that capacitive loads often cause oscillations is shown by the way that so many voltage references oscillate when loaded with large capacitors. The buffer amplifiers in voltage references could be made stable under capacitive load, but too often they are not.)

Figure 1.50 shows two methods for stabilizing an op amp driving a capaci-

tive load. In each case a series resistor is used for compensation. The resistor is placed outside the feedback loop in the first method (this is commonly referred to as open-loop compensation). This introduces a gain error at the output load because of the resulting attenuator formed by R_L and R_S . The resistor is placed inside the feedback loop in the second method (in-loop or closed-loop compensation). DC feedback is taken from the load, but AC feedback from the op amp output. This introduces AC gain errors, but is simple and eliminates DC gain error. Both methods result in loss of total bandwidth.

DRIVING CAPACITIVE LOADS

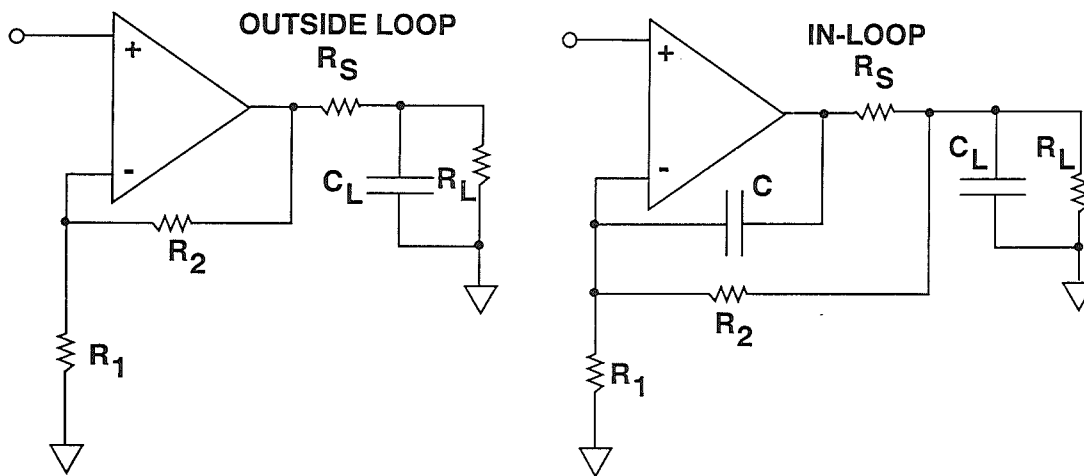
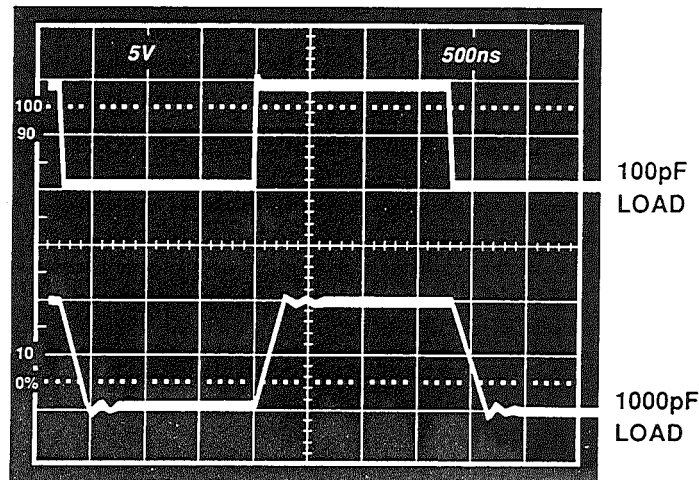


Figure 1.50

Another solution is to design an op amp whose load capacity contributes to the dominant pole of its overall response - as the load capacity increases the device slows down but remains stable. The AD817/AD847 family of op

amps uses this principle (see Reference 7). Pulse response for two capacitive loads is shown in Figure 1.51. Note that increasing the load capacitance from 100pF to 1000pF reduces the bandwidth proportionally.

LOAD CAPACITANCE CONTRIBUTES TO DOMINANT POLE IN AD847 OP AMP



VERTICAL SCALE: 5V/div.
HORIZONTAL SCALE: 500ns/div.

Figure 1.51

Frequency Response - Voltage Feedback Op amps - Gain-Bandwidth Products

The open-loop frequency response of a voltage feedback op amp is shown in Figure 1.52. There are two possibilities: the left-hand diagram shows the most common, where a high DC gain drops at 6 dB/octave from quite a low frequency down to unity gain. This is a single pole response. The amplifier in the right-hand diagram has two poles in its

response - the gain drops at 6 dB/octave for a while and then drops at 12 dB/octave. The amplifier in the left-hand diagram is known as an *unconditionally stable* or *fully compensated* type and may be used with a noise gain of unity. They are stable with 100% feedback (including capacitance) from output to inverting input.

FREQUENCY RESPONSE OF VOLTAGE FEEDBACK OP AMPS

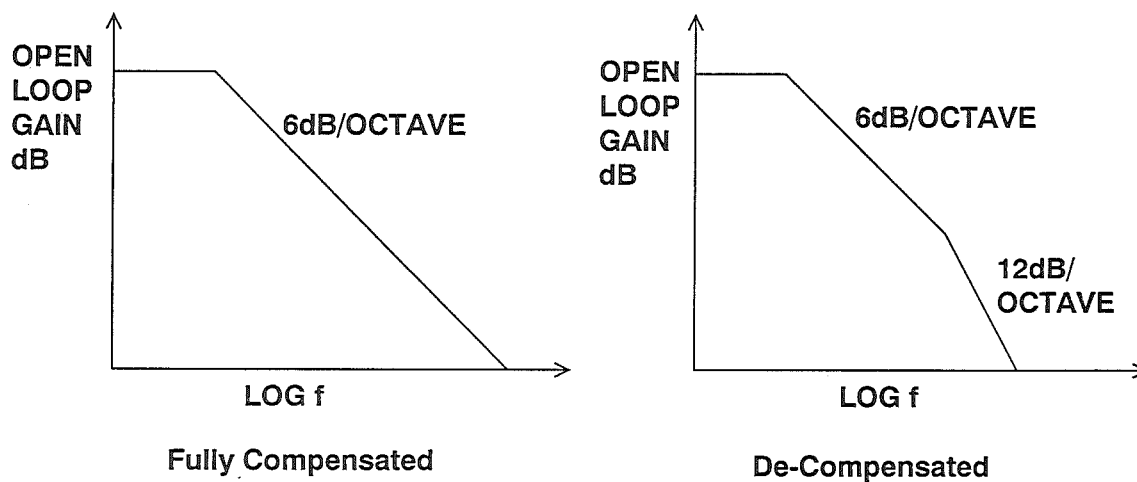


Figure 1.52

If the amplifier in the right-hand diagram is used with a noise gain which is lower than the gain at which the slope of the response increases from 6 to 12dB/octave, the phase shift in the feedback will be too great, and it will oscillate. Amplifiers of this type are characterized as “stable at gains $\geq X$ ” where X is the gain at the frequency where the 6dB/12dB transition occurs. It is, of course, the noise gain which is

referred to, and it will generally be between 2 and 25. These *decompensated* op amps have higher gain-bandwidth products than fully compensated amplifiers, all other things being equal, and so are useful despite the slightly greater complication of designing with them. They can never be used with direct capacitive feedback from output to inverting input.

The 6dB/octave slope of the response of both types means that over the range of frequencies where it occurs, the product of the closed-loop gain and the 3dB closed-loop bandwidth at that gain is a constant - this is known as the *gain-bandwidth product* (GBW) and is a figure of merit for an amplifier. If an op amp has a GBW product of X MHz,

then its closed loop bandwidth at a noise gain of 1 will be X MHz, at a noise gain of 2 it will be X/2 MHz, and at a noise gain of Y it will be X/Y MHz (see Figure 1.53). Notice that the *closed-loop bandwidth* is the frequency at which the noise gain intersects the open-loop gain.

GAIN-BANDWIDTH PRODUCT FOR VOLTAGE FEEDBACK OP AMPS

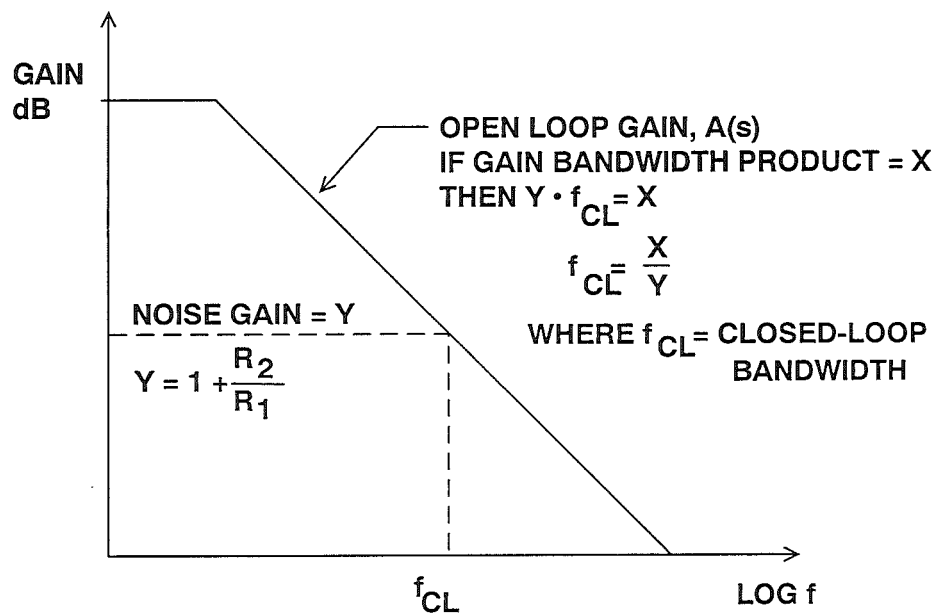


Figure 1.53

In the above example, we assumed that the feedback elements were resistive. This is not usually the case, especially when the op amp requires a feedback capacitor for stability. Figure 1.54 shows a typical example where there is capacitance, C1, on the inverting input of the op amp. The capacitance is the sum of the op amp internal capacitance and any external capacitance which may exist. This capacitance introduces a pole in the noise gain transfer function. Stability of the system is deter-

mined by the net slope of the noise gain and the open-loop gain where they intersect. For unconditional stability, the noise gain must intersect the open-loop gain with a net slope of less than 12dB/octave (20dB per decade). Adding the feedback capacitor, C2, introduces a zero in the noise gain transfer function which stabilizes the circuit. Notice that the closed-loop bandwidth, f_{CL} , is determined by the frequency at which the noise gain intersects the open-loop gain.

BODE PLOT SHOWING NOISE GAIN FOR VOLTAGE FEEDBACK OP AMP WITH REACTIVE ELEMENTS

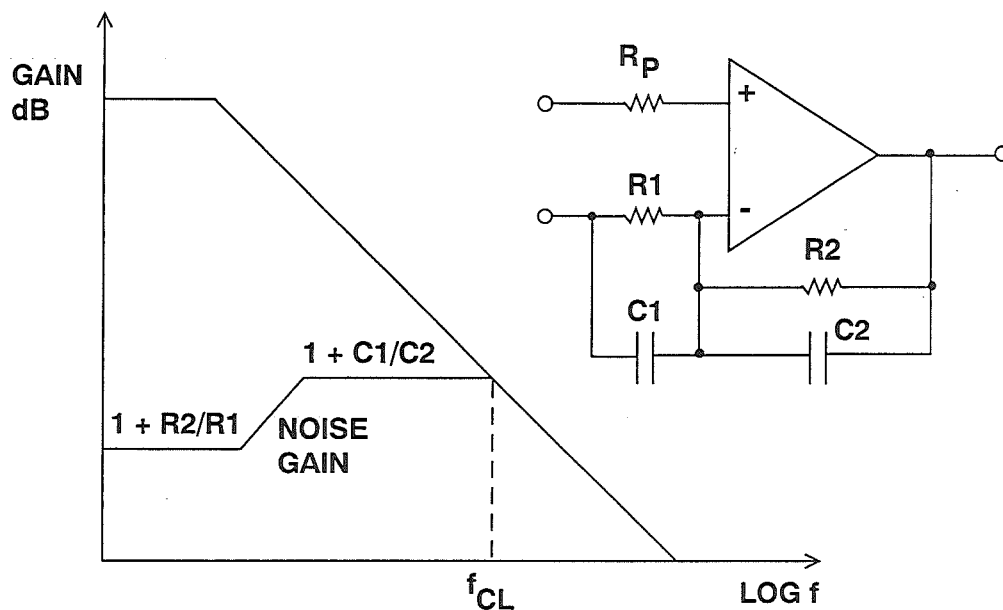


Figure 1.54

The Bode Plot of the noise gain is a very useful tool in analyzing op amp stability. Constructing the Bode plot is a relatively simple matter. Although it is

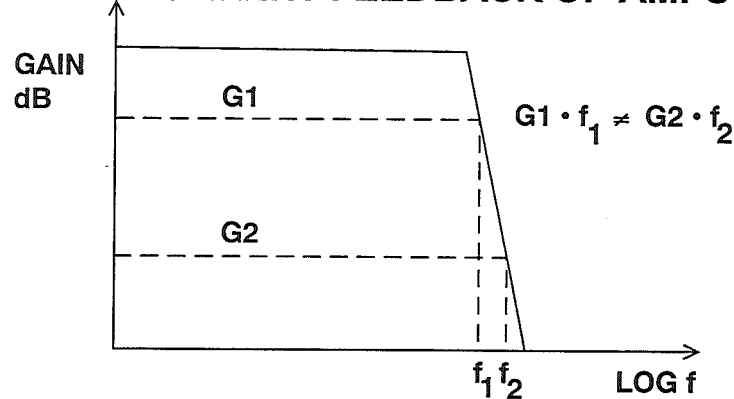
outside the scope of this section to carry the discussion of noise gain and stability further, the reader is referred to Reference 5.

Frequency Response - Current Feedback Op amps

Current feedback op amps do not behave in the same way as voltage feedback types. They are rarely stable with capacitive feedback, or with a short circuit from output to inverting input. There is generally an optimum feedback resistance for maximum bandwidth (the value of this resistance may vary with supply voltage - consult individual device data sheets). If the feedback resistance is increased, the bandwidth is reduced. If it is reduced, the bandwidth increases, and the amplifier may become unstable.

But for a given value of feedback resistance (R_2), the bandwidth is largely unaffected by the noise gain. It is therefore incorrect to refer to the gain-bandwidth product of a current feedback amplifier. If R_1 is too large, its shunt capacitance affects gain, and if it is too small (comparable to the actual input resistance of the amplifier on its inverting input), the interaction of the two is troublesome.

FREQUENCY RESPONSE FOR CURRENT FEEDBACK OP AMPS



- Feedback resistor fixed for optimum performance.
Larger values reduce bandwidth, smaller values may cause instability.
- For fixed feedback resistor, changing gain has little effect on bandwidth.
- Current feedback op amps do not have a fixed gain-bandwidth product.

Figure 1.55

When used in the inverting mode, with the non-inverting input grounded, noise gains of little more than unity (signal gains $\ll 1$) are possible with current feedback amplifiers. In the non-inverting mode, however, the minimum value of the resistor from the output to the inverting input reacts with stray capacitance on the inverting input to attenuate feedback at HF and produce gain peaking. General purpose current feedback amplifiers generally do

not have very flat frequency response when used in the non-inverting mode at low gains unless specifically designed for this application. The AD811 video op amp was optimized for bandwidth flatness (0.1dB from DC to 30MHz) for a gain of two and a resistive termination of 150Ω (75Ω source and load-terminated cable). However, a few pF of stray capacitance on the output will cause gain peaking even with this amplifier.

FREQUENCY RESPONSE FOR CURRENT FEEDBACK OP AMPS

- Stray capacitance (either on inverting input or output or both) may cause gain peaking especially at low gains in non-inverting mode with minimum value of feedback resistor
- Bandwidth is relatively independent of gain for fixed feedback resistor
- High gains in inverting mode may be impractical because of low value feedforward resistor
- Current feedback op amps may be optimized for flat frequency response at low gains with no capacitive loading (AD811)

Figure 1.56

Operational Amplifier Noise

This section discusses the noise generated within op amps, not external noise which they may pick up. External noise is important, and is discussed in detail in References 6 and 7, but in this section we are concerned solely with internal noise.

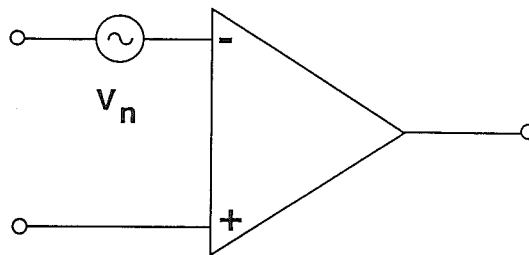
There are three noise sources in an op amp: a voltage noise which appears differentially across the two inputs, and a current noise in each input. These are effectively uncorrelated (independent of each other). In fact, there is a slight correlation between the two noise

currents, but it is too small to need consideration in practical noise analyses. In addition to these three internal noise sources, it is necessary to consider the Johnson noise of the external resistors which are used with the op amp.

All resistors have a Johnson noise of

$\sqrt{4kTBR}$, where k is Boltzmann's Constant ($1.38 \times 10^{-23} \text{ J/K}$), T is the absolute temperature, B is the bandwidth and R is the resistance. This is intrinsic - it is not possible to obtain resistors which do not have Johnson noise.

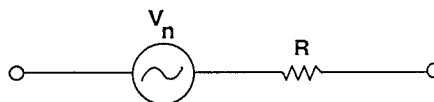
INPUT VOLTAGE NOISE



- Input Voltage Noise is bandwidth dependent and measured in $\text{nV}/\sqrt{\text{Hz}}$ (spectral density)
- Normal Ranges are $1\text{nV}/\sqrt{\text{Hz}}$ to $20\text{nV}/\sqrt{\text{Hz}}$

Figure 1.57

JOHNSON NOISE OF RESISTORS



- ALL resistors have a voltage noise of $\sqrt{4kTBR}$
- T = Absolute Temperature = $T(^{\circ}\text{C}) + 273.15$
- B = Bandwidth (Hz)
- k = Boltzmann's Constant ($1.38 \times 10^{-23} \text{J/K}$)
- A 1000Ω resistor generates $4\text{nV}/\sqrt{\text{Hz}}$ @ 25°C

Figure 1.58

Uncorrelated noise voltages add in a "root sum of squares" manner; i.e., noise voltages V_1 , V_2 , V_3 give a result of

$$\sqrt{V_1^2 + V_2^2 + V_3^2}.$$

Noise powers, of course, add normally. Thus, any noise voltage which is more than 4 or 5 times any of the others is dominant, and the others may generally be ignored. This simplifies noise assessment.

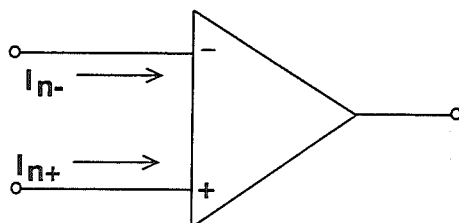
The voltage noise of different op amps may vary from under 1 nV/√Hz to 20 nV/√Hz, or even more. Bipolar op amps tend to have lower voltage noise than JFET ones, although it is possible to make JFET op amps with low voltage noise (such as the AD743/AD745), at the cost of large input devices and hence large (~20 pF) input capacitance. Voltage noise is normally specified on the

data sheet, and it is not possible to predict it from other parameters.

Current noise can vary much more widely, from around 0.1 fA/√Hz (in JFET electrometer op amps) to several pA/√Hz (in high speed bipolar op amps). It is not always specified on data sheets, but may be calculated in cases (like simple BJT or JFET input devices) where all the bias current flows in the input junction, because in these cases it is simply the Schottky (or shot) noise of the bias current. It cannot be calculated for bias-compensated or current feedback op amps, where the external bias current is the *difference* of two internal current sources. The shot noise spectral

density is simply $\sqrt{2I_b q}$ amps/√Hz, where I_b is the bias current (in amps) and q is the charge on an electron (1.6×10^{-19} C).

INPUT CURRENT NOISE



- Normal Ranges: 0.1fA/√Hz to 10pA/√Hz
- In Voltage Feedback op amps the current noise in the inverting and non-inverting inputs is uncorrelated (effectively) but roughly equal in magnitude.
- In simple BJT and JFET input stages, the current noise is the shot noise of the bias current and may be calculated from the bias current.
- In bias-compensated input stages and in current feedback op amps, the current noise cannot be calculated.
- The current noise in the two inputs of a current feedback op amp may be quite different. It may not even have the same 1/f corner.

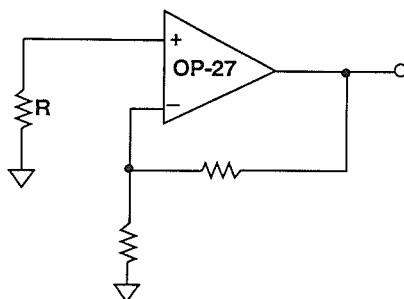
Figure 1.59

Current noise is only important when it flows in an impedance and generates a noise voltage. Therefore, the choice of a low noise op amp depends on the impedances around it. Consider an OP-27, a bias compensated op amp with low voltage noise ($3\text{nV}/\sqrt{\text{Hz}}$), but quite high current noise ($1\text{pA}/\sqrt{\text{Hz}}$). With zero source impedance, the voltage noise will dominate as shown in Figure 1.60. With a source resistance of $3\text{k}\Omega$, the current noise ($1\text{pA}/\sqrt{\text{Hz}}$ flowing in $3\text{k}\Omega$) will

equal the voltage noise, but the Johnson noise of the $3\text{k}\Omega$ resistor is $7\text{nV}/\sqrt{\text{Hz}}$ and so is dominant. With a source resistance of $300\text{k}\Omega$, the current noise increases a hundredfold to $300\text{nV}/\sqrt{\text{Hz}}$, while the voltage noise continues unchanged, and the Johnson noise (which is proportional to the *square root* of the resistance) only increases tenfold. Here, current noise is dominant.

EFFECT OF SOURCE RESISTANCE ON TOTAL NOISE REFERRED TO INPUT

Example: OP-27
Voltage Noise = $3\text{nV}/\sqrt{\text{Hz}}$
Current Noise = $1\text{pA}/\sqrt{\text{Hz}}$
($T = 25^\circ\text{C}$)



CONTRIBUTION FROM	VALUES OF R		
	0	$3\text{k}\Omega$	$300\text{k}\Omega$
AMPLIFIER VOLTAGE NOISE	3	3	3
AMPLIFIER CURRENT NOISE FLOWING IN R	0	3	300
JOHNSON NOISE OF R	0	7	70

RTI NOISE ($\text{nV}/\sqrt{\text{Hz}}$)
Dominant Noise is Highlighted

Figure 1.60

The above example shows that the choice of a low noise op amp depends on the source impedance of the signal, and at high impedances, current noise always dominates.

For low impedance circuitry, amplifiers with low voltage noise, such as the OP-27, will be the obvious choice, since they are inexpensive, and their comparatively large current noise will not affect the application (see Figure 1.61). At

medium resistances, the Johnson noise of resistors is dominant, while at very high resistances, we must choose an op amp with the smallest possible current noise, such as the AD549 or AD645.

Until recently, BiFET amplifiers tended to have comparatively high voltage noise (though very low current noise), and were thus more suitable for low noise applications in high rather than low impedance circuitry. The AD645

and AD743/AD745 have very low values of both voltage and current noise. The AD645 specifications at 10kHz are 10nV/√Hz and 0.6fA/√Hz, and the AD743/AD745 specifications at

10kHz are 2.9nV/√Hz and 6.9fA/√Hz. These make possible the design of low-noise amplifier circuits which have low noise over a wide range of source impedances.

DIFFERENT AMPLIFIERS ARE BEST AT DIFFERENT IMPEDANCE LEVELS

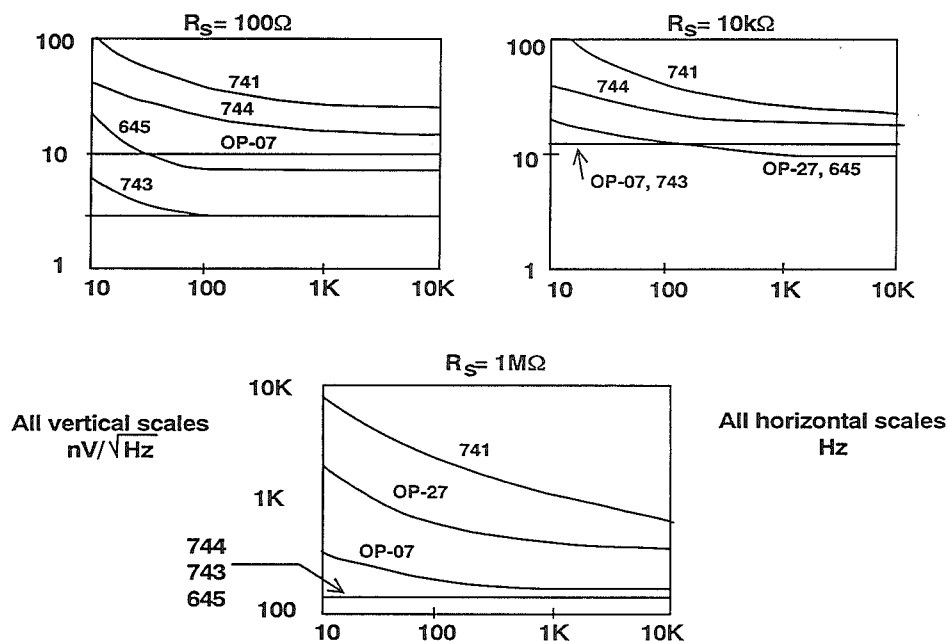


Figure 1.61

The *noise figure* of an amplifier is the amount (in dB) by which the noise of the amplifier exceeds the noise of a perfect noise-free amplifier in the same environment. The concept is useful in RF and TV applications, where 50Ω and 75Ω transmission lines and terminations are ubiquitous, but is useless for an op amp which may be used in a wide variety of electronic environments. Voltage noise spectral density and current noise spectral density are more useful specifications.

So far, we have assumed that noise is white (i.e., its spectral density does not

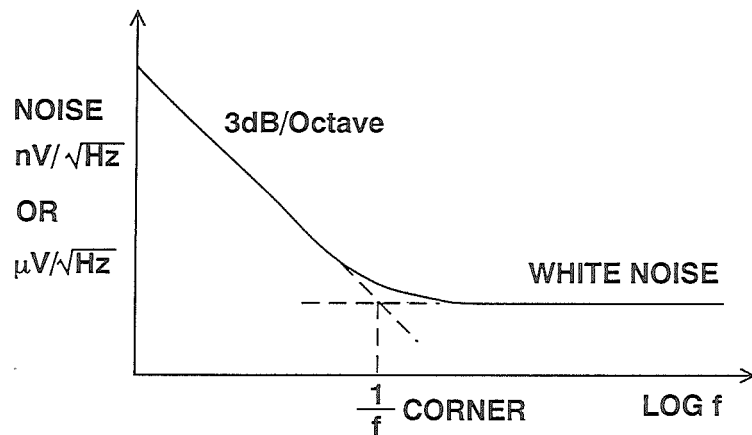
vary with frequency). This is true over most of an op amp's frequency range, but at low frequencies the noise spectral density rises at 3dB/octave as shown in Figure 1.63. The frequency at which it starts to rise is known as the 1/f corner frequency and is a figure of merit - the lower the better. The 1/f corner frequencies are not necessarily the same for the voltage noise and the current noise of a particular amplifier, and a current feedback op amp may have three 1/f corners: for its voltage noise, its inverting input current noise, and its non-inverting input current noise.

NOISE FIGURE

- The *Noise Figure* of an amplifier in a particular circuit is the amount by which the noise of that circuit exceeds that of the same circuit when using a noise-free amplifier.
- Noise Figure is always specified at a particular source resistance (usually 50 or 75Ω)
- It is generally given in dB
- It is a somewhat useless concept for op amps, as they are used in too wide a range of environments

Figure 1.62

FREQUENCY CHARACTERISTICS OF OP AMP NOISE



- $1/f$ Corner Frequency is a figure of merit for op amp noise performance (the lower the better)
- Typical Ranges: 2Hz to 2kHz
- Voltage Noise and Current Noise do not necessarily have the same $1/f$ corner frequency

Figure 1.63

The best low frequency low noise amplifiers have corner frequencies in the range 1-10Hz, while JFET devices and more general purpose op amps have values in the range to 100Hz. Very fast amplifiers, however, may make compromises in processing to achieve high

speed which result in quite poor 1/f corners of several hundred Hz or even 1-2kHz. This is generally unimportant in the applications for which they were intended, but may affect their use at audio frequencies.

RMS Noise Considerations

As was discussed above, noise spectral density is a function of frequency. In order to obtain the RMS noise, the noise spectral density curve must be integrated over the bandwidth of interest.

In the 1/f region, the RMS noise in the bandwidth f_1 to f_2 is given by

$$e_{\text{rms}} = \sqrt{\int_{f_1}^{f_2} \frac{df}{f}} = k \sqrt{\ln \frac{f_2}{f_1}}$$

where k is the noise spectral density at 1Hz. The total 1/f noise in a given band

is a function of the ratio of the low and high band edge frequencies, since the actual frequency cancels out. It is necessary, however, that the upper band edge is still in the 1/f region for the above formula to be accurate.

In many cases, the low frequency noise is specified as a peak-to-peak value within the bandwidth 0.1 to 10Hz. This is measured by inserting a 0.1 to 10Hz bandpass filter between the op amp and the measuring device. The measurement is often presented as a scope photo with a time scale of 1s/div as shown in Figure 1.64 for the OP-213.

THE 1/f NOISE IN THE BANDWIDTH 0.1Hz TO 10Hz IS LESS THAN 120nV PEAK-TO-PEAK FOR THE OP-213

SCALES

VERTICAL:
20nV/div.

HORIZONTAL:
1s/div.

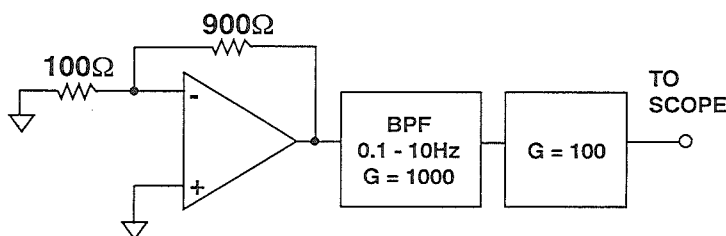
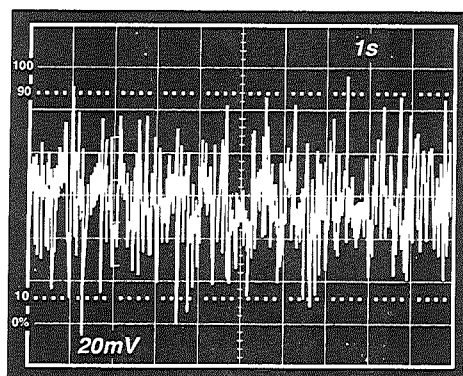


Figure 1.64

In practice, it is virtually impossible to measure noise within specific frequency limits with no contribution from outside those limits, since practical filters have finite rolloff characteristics. Fortunately, the measurement error introduced by a single pole lowpass filter is readily computed. The noise in the spectrum above the single pole filter cutoff frequency, f_c , extends the corner

frequency to $1.57f_c$. Similarly, a two pole filter has an apparent corner frequency of approximately $1.2f_c$. The error correction factor is usually negligible for filters having more than two poles. The bandwidth obtained after applying the correction factor is referred to as the *equivalent noise bandwidth* of the filter (see Figure 1.65).

EQUIVALENT NOISE BANDWIDTH

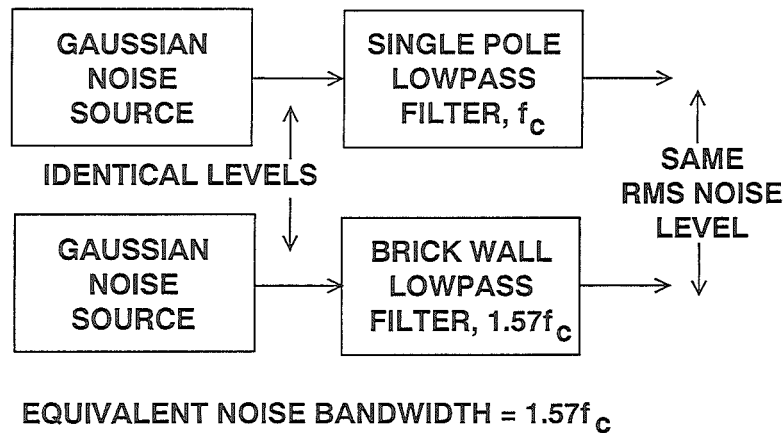


Figure 1.65

When computing RMS noise for wide bandwidth op amps, $1/f$ noise becomes relatively insignificant. The dominant source of noise is *gaussian*, or white noise. This noise has a relatively constant noise spectral density over a wide range of frequencies. The RMS noise calculation is made by multiplying the noise spectral density by the square root of the equivalent noise bandwidth.

It is often desirable to convert RMS noise measurements into peak-to-peak. In order to do this, one must have some understanding of the statistical nature of noise. For Gaussian noise

and a given value of RMS noise, statistics tell us that the chance of a particular peak-to-peak value being exceeded decreases sharply as that value increases - but this probability never becomes zero. Thus, for a given RMS noise, it is possible to predict the percentage of time that a given peak-to-peak value will be exceeded, but it is not possible to give a peak-to-peak value which will never be exceeded (see Figure 1.66). Peak-to-peak noise specifications, therefore, must always be written with a time limit. A suitable one is 6.6 times the RMS value which is exceeded only 0.1% of the time.

RMS TO PEAK-TO-PEAK RATIOS

Nominal Peak-to-Peak	% of the Time Noise will Exceed Nominal Peak-to-Peak Value
$2 \times \text{rms}$	32%
$3 \times \text{rms}$	13%
$4 \times \text{rms}$	4.6%
$5 \times \text{rms}$	1.2%
$6 \times \text{rms}$	0.27%
$6.6 \times \text{rms}^{**}$	0.10%
$7 \times \text{rms}$	0.046%
$8 \times \text{rms}$	0.006%

**** Most often used conversion factor is 6.6**

Figure 1.66

Total Output Noise Calculations

We have already pointed out that any noise source which produces less than one third to one fifth of the noise of some other source can be ignored. (Both noise voltages must be measured at the same point in the circuit.) To analyze the noise performance of an op amp circuit, we must assess the noise contributions of each part of the circuit and determine which are significant. To simplify the following calculations, we shall work with noise spectral densities, rather than actual voltages, to leave bandwidth out of the expressions (the noise spectral density, which is generally expressed in $\mu\text{V}/\sqrt{\text{Hz}}$, is equivalent to the noise in a 1 Hz bandwidth).

If we consider the circuit in Figure 1.67, which is an amplifier consisting of an op amp and three resistors (R_p represents the source resistance at node A), we can find six separate noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the op amp. Each has its own contribution to the noise at the amplifier output. (Noise is generally specified RTI, or *referred to the input*, but it is often simpler to calculate the noise at the output and then divide it by the *signal* gain (not the *noise* gain) of the amplifier to obtain the RTI noise).

OP AMP NOISE MODEL SHOWING REACTIVE ELEMENTS

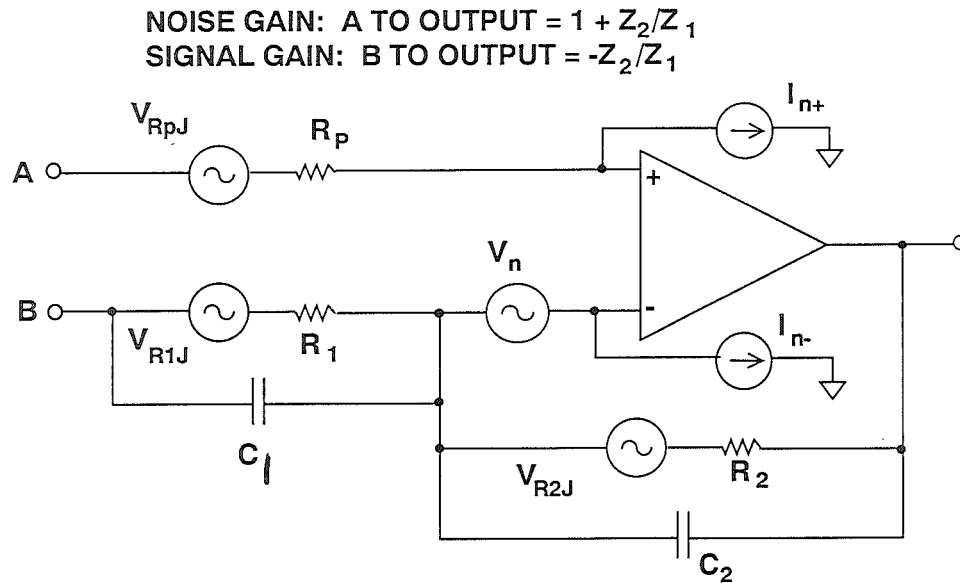


Figure 1.67

The circuit represents a second-order system, where capacitor C_1 represents the source capacitance, stray capacitance on the inverting input, the input capacitance of the op amp, or any combination of these. C_1 causes a breakpoint in the noise gain, and C_2 is

the capacitor which must be added to obtain stability. Because of C_1 and C_2 , the noise gain is a function of frequency, and has peaking at the higher frequencies (assuming C_2 is selected to make the second-order system critically damped).

A DC signal applied to input A (B being grounded) sees a gain of:

$$1 + R_2/R_1 = \text{DC Noise Gain} \quad [1a]$$

At higher frequencies, the gain from input A to the output becomes:

$$1 + C_2/C_1 = \text{AC Noise Gain} \quad [1b]$$

The closed-loop bandwidth f_{cl} is the point at which the Noise Gain intersects the open-loop gain.

A DC signal applied to B (A being grounded) sees a gain of:

$$-R_2/R_1 \quad [2a]$$

with a high frequency cutoff determined by R_2C_2 :

$$\text{Bandwidth (B to Output)} = 1/2\pi R_2C_2 \quad [2b]$$

These are the non-inverting and inverting gains and bandwidths, respectively, of the amplifier.

The current noise of the non-inverting input, I_{n+} , flows in R_p and gives rise to a noise voltage of $I_{n+}R_p$, which is amplified by [1a, 1b], as are the op amp noise voltage, V_n , and the Johnson

noise of R_p , which is $\sqrt{4kTR_p}$. The Johnson noise of R_1 is amplified by [2a] over a bandwidth of $1/2\pi R_2 C_2$ [2b], and the Johnson noise of R_2 is not amplified at all but is buffered directly to the output over a bandwidth of $1/2\pi R_2 C_2$. The current noise of the inverting input, I_{n-} , does not flow in R_1 , as might be expected - negative feedback around the amplifier works to keep the potential at the inverting input unchanged, so that a current flowing from that pin is forced, by negative feedback, to flow in R_2 only, resulting in a voltage at the amplifier output of $I_{n-}R_2$ over a bandwidth of $1/2\pi R_2 C_2$ (we could equally well consider the voltage caused by I_{n-} flowing in the parallel combination of R_1 & R_2 and then amplified by the noise gain of the amplifier (see below), but the results are identical — only the calculations are more involved).

If we consider these six noise contributions, we see that if R_p and R_2 are low, then the effect of current noise and Johnson noise will be minimized, and the dominant noise will be the op amp's voltage noise. As we increase resistance, both Johnson noise and the voltage noise produced by noise currents will rise. If noise currents are low, then Johnson noise will take over from voltage noise as the dominant contributor. Johnson noise, however, rises with the square root of the resistance, while the current noise voltage rises linearly

with resistance, so ultimately, as the resistance continues to rise, the voltage due to noise currents will become dominant.

These noise contributions we have analyzed are not affected by whether the input is connected to node A or node B (the other being grounded or connected to some other low-impedance voltage source), which is why the non-inverting gain $(1 + R_2/R_1)$, which is seen by the voltage noise of the op amp, V_n , is known as the "noise gain" of the amplifier.

Calculating the total output RMS noise of the op amp requires multiplying each of the six noise voltages by the appropriate gain and integrating over the appropriate frequency as shown in Figure 1.68. The root-sum-square of all the output contributions then represents the total RMS output noise. Fortunately, this cumbersome exercise may be greatly simplified in most cases by making the appropriate assumptions.

The noise gain for a typical second-order system is shown in Figure 1.69. It is quite easy to perform the voltage noise integration in two steps, but notice that because of peaking, the majority of the output noise due to the input voltage noise will be determined by the high frequency portion where the noise gain is $1 + C_1/C_2$. This type of response is typical of second-order systems. The noise due to the inverting input current noise, R_1 , and R_2 is only integrated over the bandwidth $1/2\pi R_2 C_2$. The appropriate model for the second-order system (neglecting resistor noise) is shown in Figure 1.70.

REFERRING ALL NOISE SOURCES TO THE OUTPUT

NOISE SOURCE EXPRESSED AS A VOLTAGE	MULTIPLY BY THIS FACTOR TO REFLECT TO OUTPUT	INTEGRATION BANDWIDTH
Johnson Noise in R_p : $\sqrt{4kTR_p}$	Noise Gain as a Function of Frequency	Closed Loop BW (Signal BW from A to Output)
Non-Inverting Input Current Noise Flowing in R_p : $I_{n+}R_p$	Noise Gain as a Function of Frequency	Closed Loop BW (Signal BW from A to Output)
Input Voltage Noise: V_n	Noise Gain as a Function of Frequency	Closed Loop BW (Signal BW from A to Output)
Johnson Noise in R_1 : $\sqrt{4kTR_1}$	$-R_2/R_1$ (Signal Gain from B to Output)	$1/2\pi R_2 C_2$ (Signal BW from B to Output)
Johnson Noise in R_2 : $\sqrt{4kTR_2}$	1	$1/2\pi R_2 C_2$ (Signal BW from B to Output)
Inverting Input Current Noise Flowing in R_2 : $I_{n-}R_2$	1	$1/2\pi R_2 C_2$ (Signal BW from B to Output)

Figure 1.68

NOISE GAIN AND INVERTING SIGNAL GAIN FOR SECOND-ORDER SYSTEM

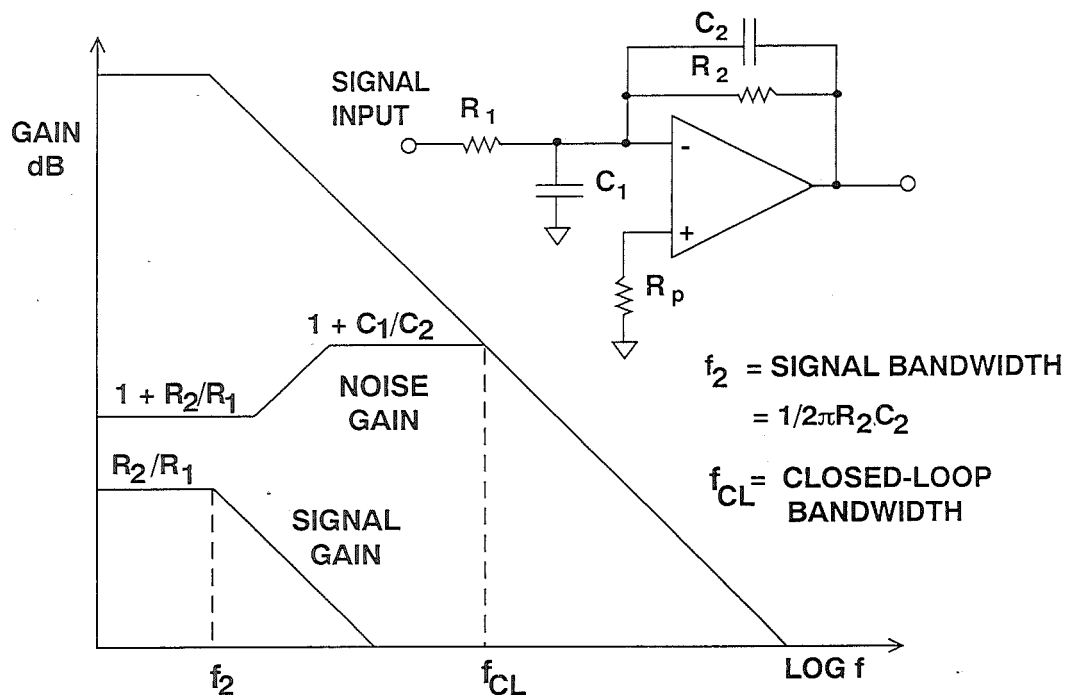
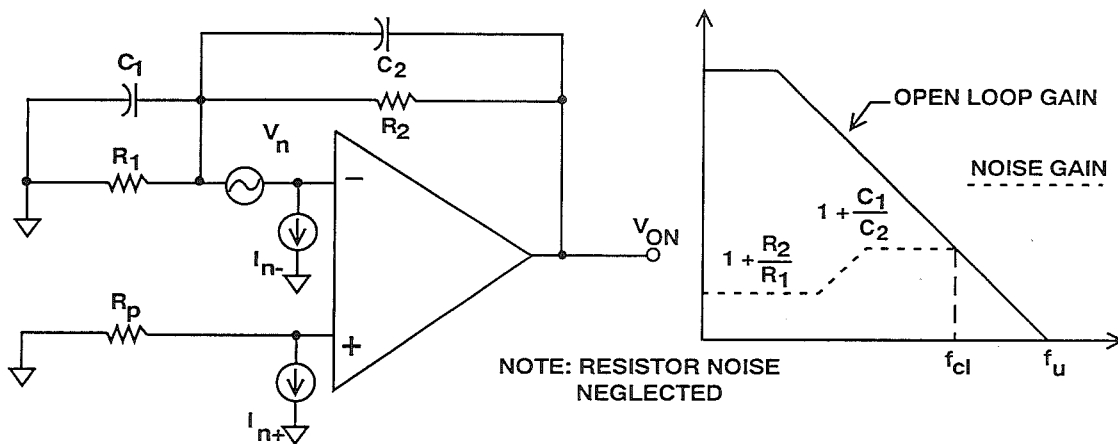


Figure 1.69

NOISE MODEL FOR A TYPICAL SECOND-ORDER SYSTEM WHICH NEGLECTS RESISTOR NOISE



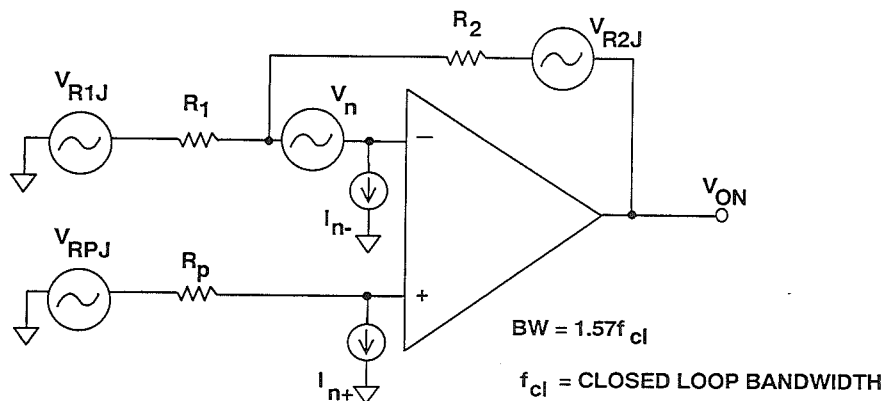
$$V_{ON} \sim \sqrt{V_n^2 \left[1 + \frac{C_1}{C_2} \right]^2 (1.57 f_{cl}) + I_{n-}^2 R_2^2 (1.57 f_2) + I_{n+}^2 R_p^2 \left[1 + \frac{C_1}{C_2} \right]^2 (1.57 f_{cl})}$$

Where f_u = Op Amp Unity Gain Bandwidth Frequency

$$f_{cl} = \text{Closed Loop Bandwidth} = \frac{f_u}{1 + \frac{C_1}{C_2}}, \quad f_2 = \text{Signal Bandwidth} = \frac{1}{2\pi R_2 C_2}$$

Figure 1.70

OP AMP NOISE MODEL FOR A FIRST-ORDER CIRCUIT WITH CONSTANT NOISE GAIN



$$V_{ON} = \sqrt{BW \left[I_{n-}^2 R_2^2 + I_{n+}^2 R_p^2 \left[1 + \frac{R_2}{R_1} \right]^2 + V_n^2 \left[1 + \frac{R_2}{R_1} \right]^2 + 4kTR_2 + 4kTR_1 \left[\frac{R_2}{R_1} \right]^2 + 4kTR_p \left[1 + \frac{R_2}{R_1} \right]^2 \right]}$$

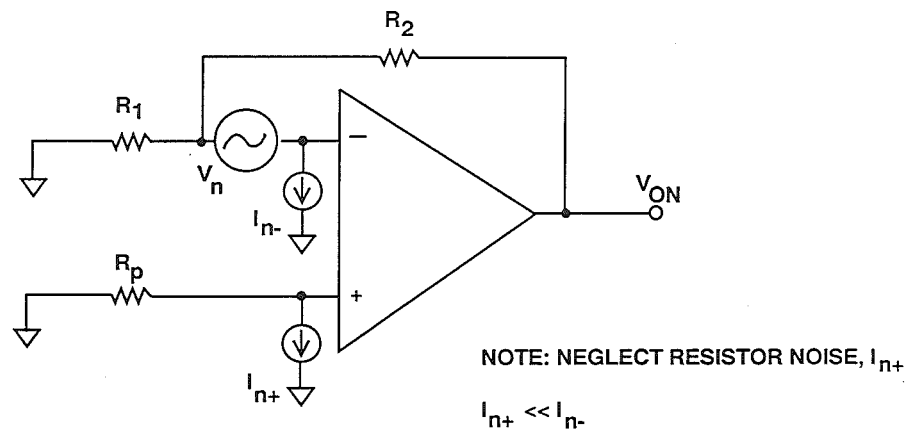
Figure 1.71

In high speed op amp applications, there are some further simplifications which can be made. The noise gain plot for a first-order system optimized for fast settling time is usually flat up to the closed-loop bandwidth frequency, with only a dB or so of gain peaking at the most. All noise sources may therefore be integrated over the closed-loop op amp bandwidth as shown in Figure

1.71. It is also safe to neglect resistor noise if feedback resistors are 1kΩ or less.

In high speed current feedback op amp circuits, the input voltage noise and the inverting input current noise are the dominant contributors to the output noise as shown in Figure 1.72.

NOISE MODEL FOR HIGH SPEED CURRENT FEEDBACK CIRCUIT



$$V_{ON} = \sqrt{1.57 f_{cl}} \sqrt{V_n^2 \left[1 + \frac{R_2}{R_1} \right]^2 + I_{n-}^2 R_2^2}$$

f_{cl} = CLOSED LOOP BANDWIDTH

Figure 1.72

Op Amp Distortion

Dynamic range of an op amp may be defined in several ways. The most common ways are to specify Harmonic Distortion, Total Harmonic Distortion (THD), or Total Harmonic Distortion Plus Noise (THD + N).

The distortion component which makes up Total Harmonic Distortion is usually

calculated by taking the root sum of the squares of the first five or six harmonics of the fundamental. In many practical situations, however, there is negligible error if only the second and third harmonics are included.

DEFINITIONS OF THD AND THD + N

- V_S = Signal Amplitude (rms Volts)
- V_2 = Second Harmonic Amplitude (rms Volts)
- V_n = nth Harmonic Amplitude (rms Volts)
- V_{noise} = rms value of noise over measurement bandwidth

- $$\text{THD} + N = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2 + V_{\text{noise}}^2}}{V_S}$$

- $$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}}{V_S}$$

Figure 1.73

It is important to note that the THD measurement does not include noise terms, while THD + N does. The noise in the THD + N measurement must be integrated over the measurement bandwidth. In audio applications, the bandwidth is normally chosen to be around 100kHz. In narrow-band applications, the level of the noise may be reduced by filtering. On the other hand, harmonics and intermodulation products which fall within the measurement bandwidth cannot be filtered, and therefore may limit the system dynamic range.

Consider the example of the simple wideband op amp circuit shown in Figure 1.74. The AD9622 is a high speed low distortion voltage feedback op amp optimized for use in a gain-of-two configuration. The input voltage noise of

3.5nV/√Hz is reflected to the output by multiplying by the noise gain, 2. The 7nV/√Hz is then integrated over the closed loop small signal bandwidth of the op amp, which is approximately 230MHz. This yields a total integrated output noise of 133μV RMS. The output noise due to the op amp input current noise and the thermal noise of the resistors is negligible in this example. The corresponding signal-to-noise ratio (neglecting distortion) for a 2V peak-to-peak sinewave output is 74.5dB. Under these conditions, however, the harmonic distortion of the AD9622 is approximately -75dBc at 2MHz. With no filtering, the dynamic range is thus equally limited by the noise and the distortion. If, however, the output of the op amp is filtered, the dynamic range is limited by the distortion.

OUTPUT NOISE AND DISTORTION OF AD9622 WIDEBAND VOLTAGE FEEDBACK OP AMP

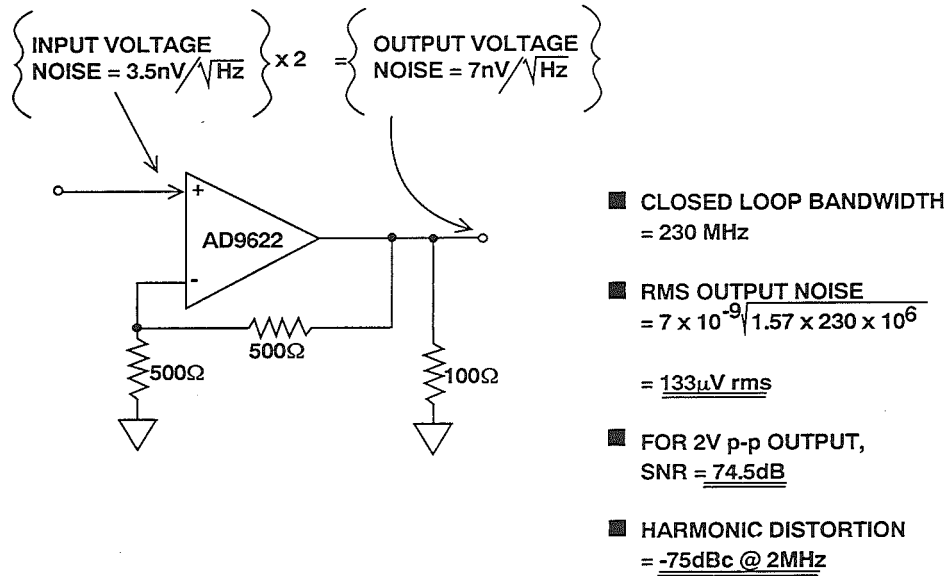


Figure 1.74

Rather than simply examining the THD produced by a single tone sinewave input, it is often useful to look at the distortion products produced by two tones. As shown in Figure 1.75, two tones will produce second and third order intermodulation products. The example shows the second and third order products produced by applying two frequencies, f_1 and f_2 , to a nonlin-

ear device. The second order products located at $f_2 + f_1$ and $f_2 - f_1$ are located far away from the two tones, and may be removed by filtering. The third order products located at $2f_1 + f_2$ and $2f_2 + f_1$ may likewise be filtered. The third order products located at $2f_1 - f_2$ and $2f_2 - f_1$, however, are close to the original tones, and filtering them is difficult.

SECOND AND THIRD-ORDER INTERMODULATION PRODUCTS FOR $f_1 = 5\text{MHz}$, $f_2 = 6\text{MHz}$

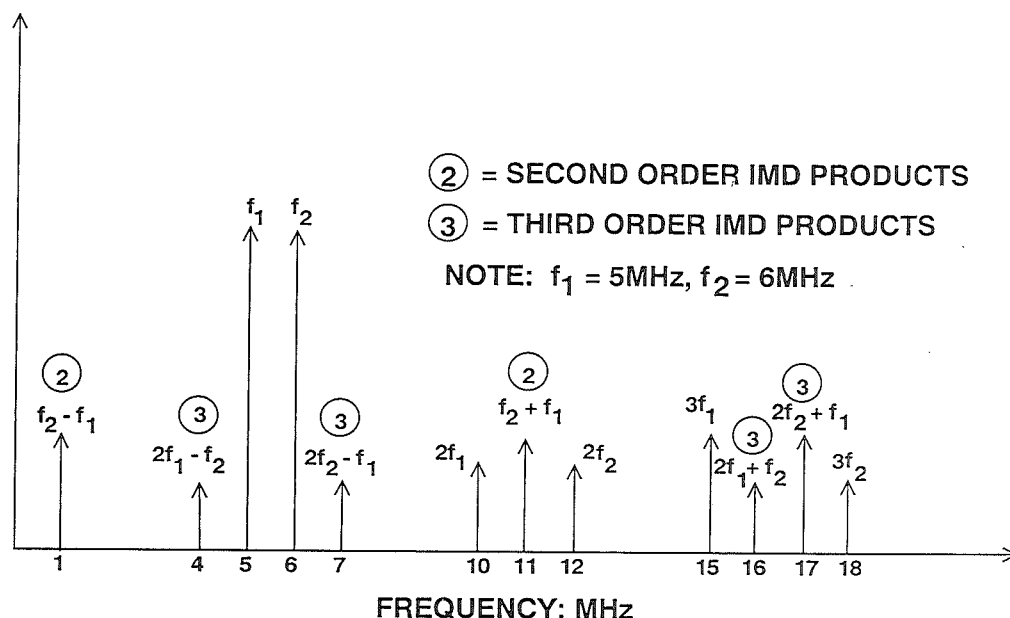


Figure 1.75

Intermodulation distortion products are of special interest in the RF area, and a major concern in the design of radio receivers. Third-order IMD products can mask out small signals in the presence of larger ones. Third order IMD is often specified in terms of the *third order intercept* point as shown in Figure 1.76. Two spectrally pure tones are applied to the system. The output signal power in a single tone (in dBm) as well as the relative amplitude of the third-order products (referenced to a single tone) is plotted as a function of input signal power. If the system non-linearity is approximated by a power series expansion, the second-order IMD amplitudes increase 2dB for every 1dB of signal increase. Similarly, the third-order IMD amplitudes increase 3dB for every 1dB of signal increase. With a low level two-tone input signal, and two data points,

draw the second and third order IMD lines as are shown in Figure 1.76, because one point and a slope determine each straight line.

Once the input reaches a certain level, however, the output signal begins to soft-limit, or compress. But the second and third-order intercept lines may be extended to intersect the extension of the output signal line. These intersections are called the *second-* and *third order intercept points*, respectively. The values are usually referenced to the output power of the device expressed in dBm. Another parameter which may be of interest is the *1dB compression point*. This is the point at which the output signal is compressed by 1dB from the ideal input/output transfer function. This point is also shown in Figure 1.76.

INTERCEPT POINTS, GAIN COMPRESSION, AND IMD

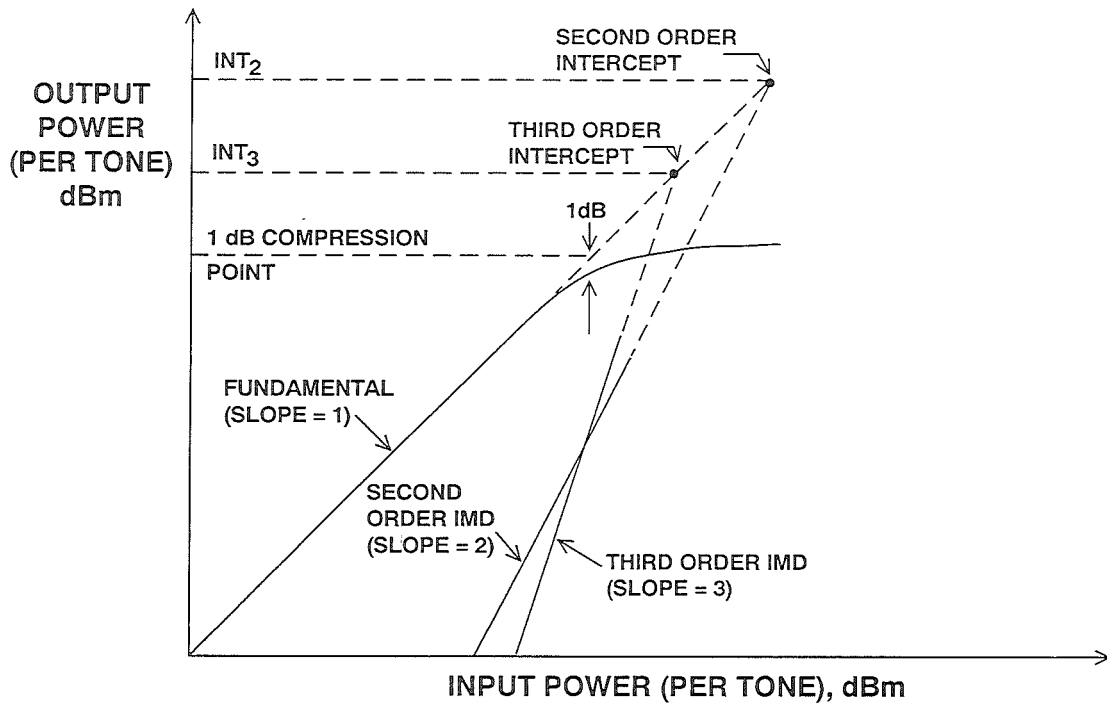


Figure 1.76

Knowing the third order intercept point allows calculation of the approximate level of the third-order IMD products as a function of output signal level. Figure

1.77 shows the third order intercept value as a function of frequency for the AD9622 voltage feedback amplifier.

AD9622 THIRD ORDER IMD INTERCEPT VERSUS FREQUENCY

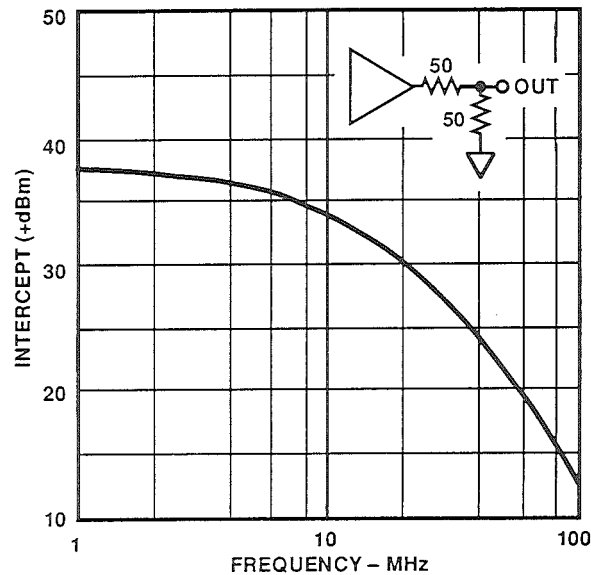


Figure 1.77

Assume the op amp output signal is 5MHz and 2V peak-to-peak into a 100Ω load (50Ω source and load termination). The voltage into the 50Ω load is therefore 1V peak-to-peak, corresponding to +4dBm. The value of the third order intercept at 5MHz is 36dBm. The difference between +36dBm and +4dBm is 32dB. This value is then multiplied

by 2 to yield 64dB (the value of the third-order intermodulation products referenced to the power in a single tone). Therefore, the intermodulation products should be -64dBc (dB below carrier frequency), or at a level of -60dBm. Figure 1.78 shows the graphical analysis for this example.

USING THE THIRD ORDER INTERCEPT POINT TO CALCULATE IMD PRODUCT FOR THE AD9622 OP AMP

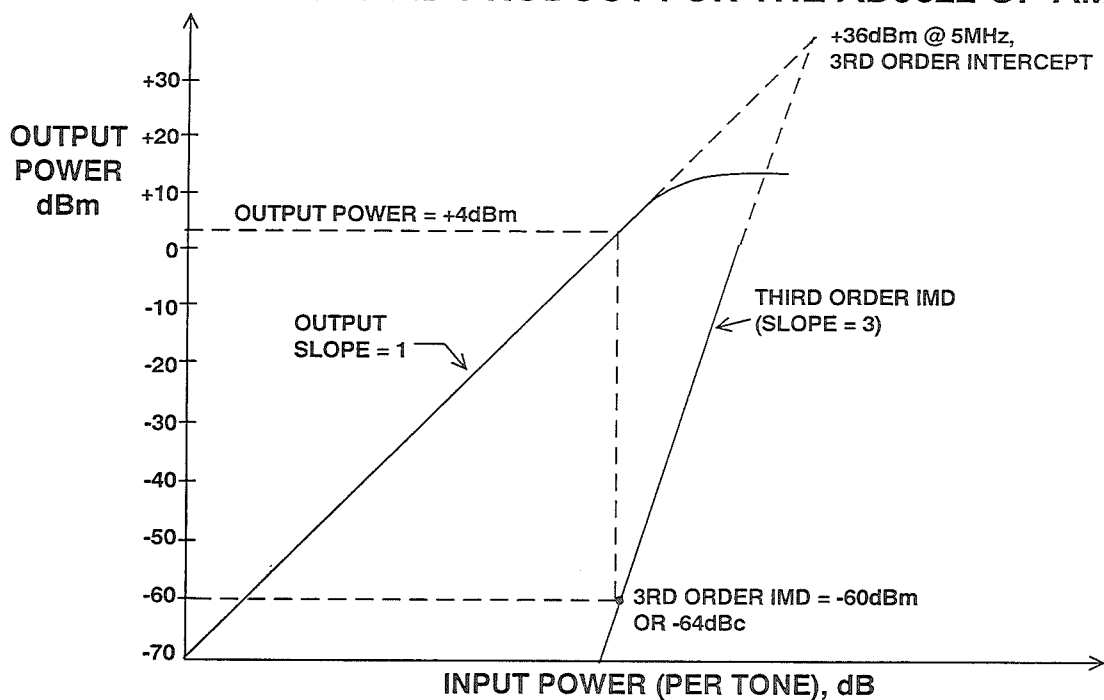


Figure 1.78

Common-Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR)

If a signal is applied equally to both inputs of an op amp, so that the differential input voltage is unaffected, the output should not be affected. In practice, changes in common-mode voltage will produce changes in output. The *common-mode rejection ratio* or CMRR is the ratio of the common-mode gain to the differential-mode gain of an op amp. For example, if a differential input change of Y volts will produce a change of 1V at the output, and a common-mode change of X volts produces a similar change of 1V, then the CMRR is X/Y . It is normally expressed in dB, and typical LF values are between 70 and 120dB. At higher frequencies, CMRR deteriorates — many op amp data sheets show a plot of CMRR versus frequency.

method shown in Figure 1.79 uses four precision resistors to configure the op amp as a differential amplifier, a signal is applied to both inputs, and the change in output is measured — an amplifier with infinite CMRR would have no change in output. The disadvantage inherent in this circuit is that the ratio match of the resistors is as important as the CMRR of the op amp. A mismatch of 0.1% between resistor pairs will result in a CMRR of only 66dB, no matter how good the op amp. Since most op amps have LF CMRRs of between 80 and 120dB, it is clear that this circuit is only marginally useful for measuring CMRR (although it does an excellent job in measuring its own resistance match!).

The common-mode rejection ratio can be measured in several ways. The

SIMPLE COMMON-MODE REJECTION RATIO (CMRR) TEST CIRCUIT

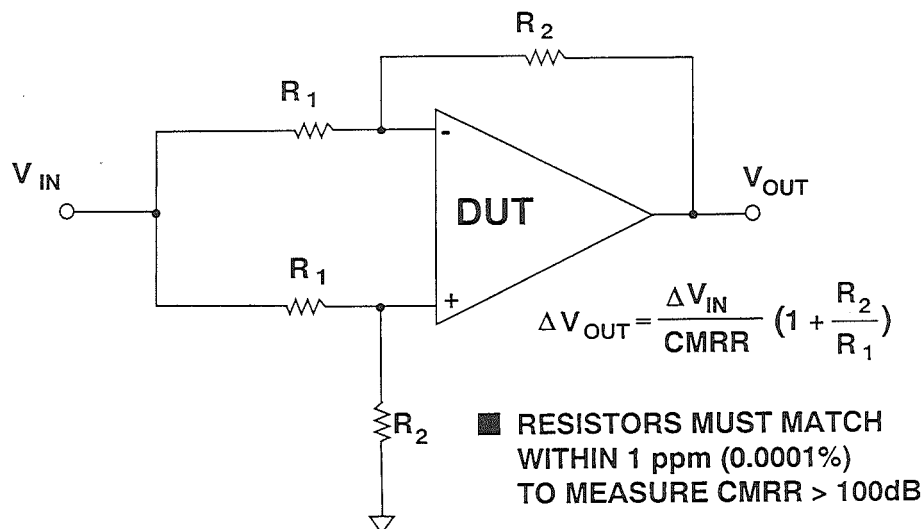


Figure 1.79

The slightly more complex circuit shown in Figure 1.80 measures CMRR without requiring accurately matched resistors. In this circuit, the common-mode voltage is changed by switching the power supply voltages. (This is easy to implement in a test facility, and the same circuit with different supply voltage connections can be used to measure

power supply rejection ratio). The power supply values shown in the circuit are for a $\pm 15V$ op amp with a common-mode voltage of $\pm 10V$. Other supplies and common-mode ranges can be accommodated by changing the voltages appropriately. The amplifier A1 should have high gain, low V_{OS} and low I_b .

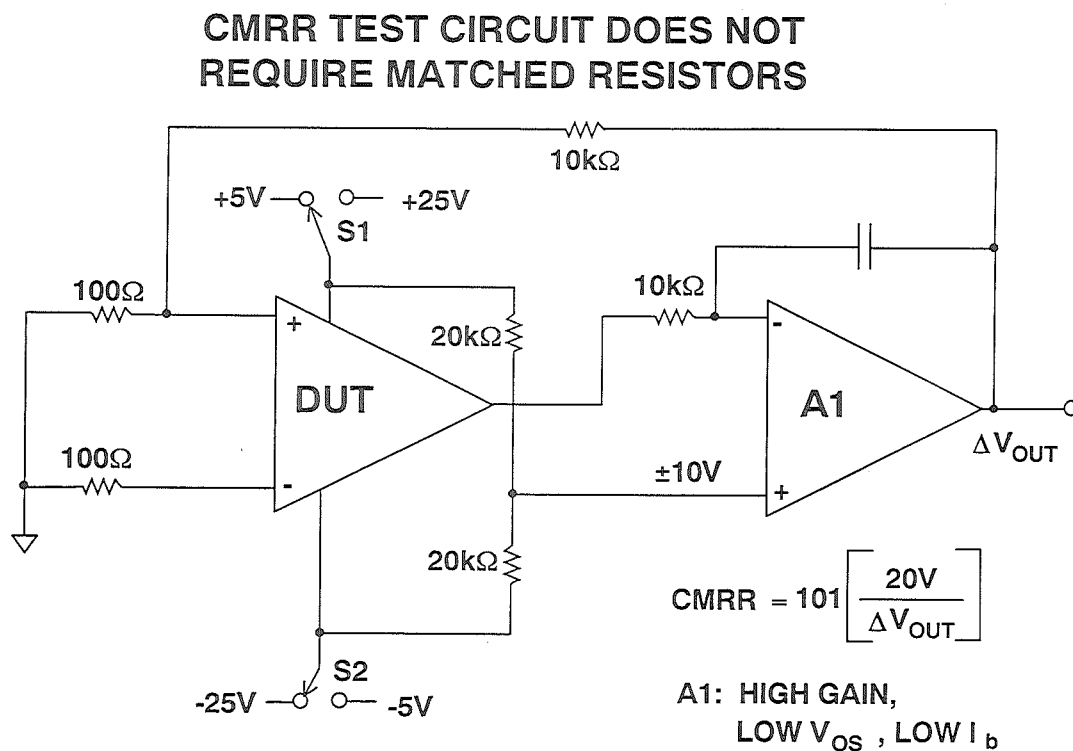


Figure 1.80

Finite CMRR produces a corresponding output offset voltage error in op amps configured in the non-inverting mode as shown in Figure 1.81. Op amps config-

ured in the inverting mode have no CMRR output error because both inputs are at ground or virtual ground, so there is no common-mode voltage.

CALCULATING OUTPUT OFFSET ERROR DUE TO CMRR

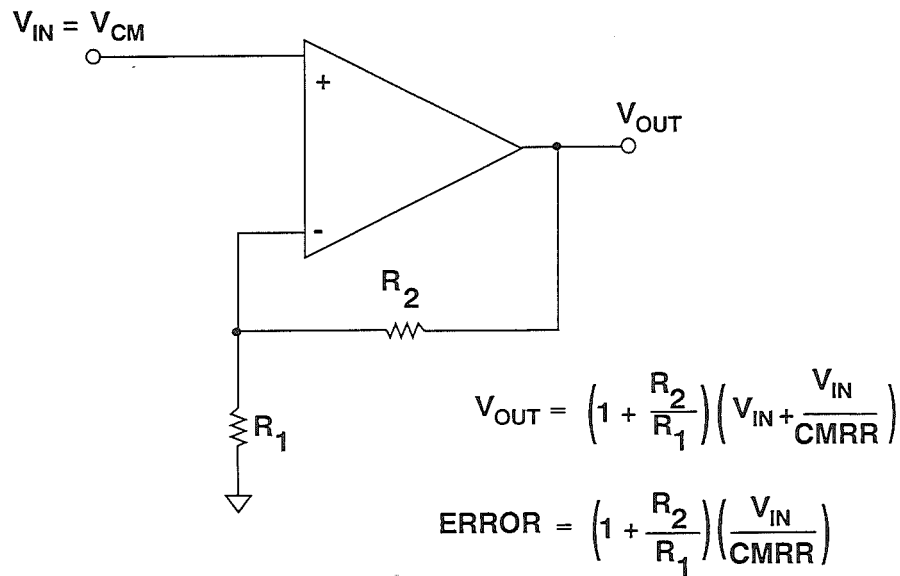


Figure 1.81

If the supply of an op amp changes, its output should not, but it does. The specification of *power supply rejection ratio* or PSRR is defined similarly to the definition of CMRR. If a change of X volts in the supply produces the same output change as a differential input change of Y volts, then the PSRR on that supply is X/Y. The definition of PSRR assumes that both supplies are altered equally in opposite directions - otherwise the change will

introduce a common-mode change as well as a supply change, and the analysis becomes considerably more complex. It is this effect which causes apparent differences in PSRR between the positive and negative supplies. The test setup used to measure CMRR may be modified to measure PSRR as shown in Figure 1.82. The voltages are chosen for a symmetrical power supply change of 1V. Other values may be used where appropriate.

TEST SETUP FOR MEASURING POWER SUPPLY REJECTION RATIO (PSRR)

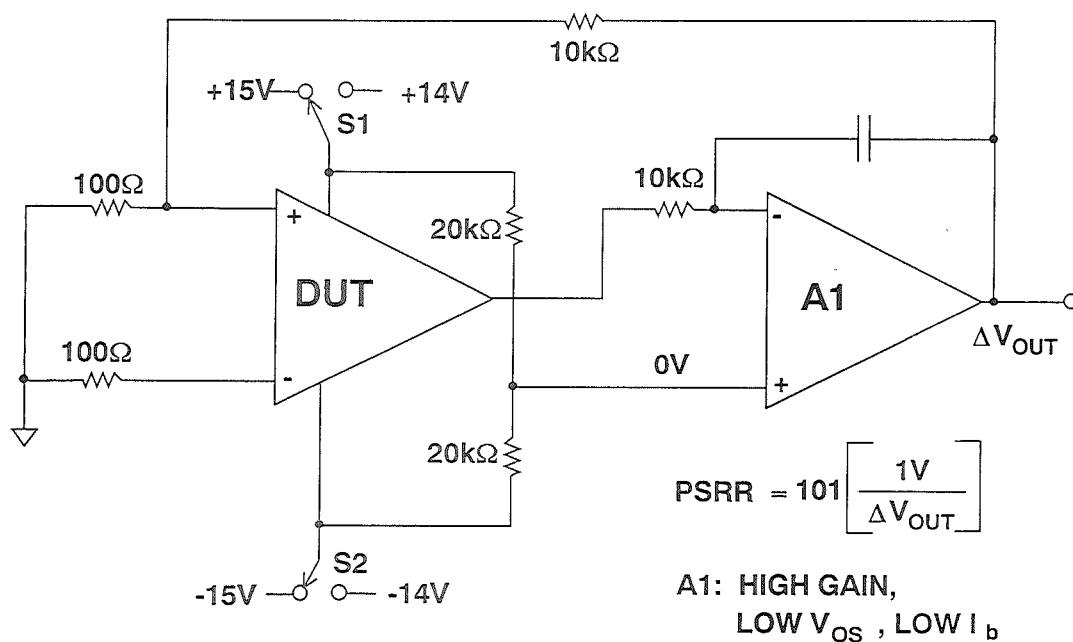


Figure 1.82

BOTH CMRR AND PSRR ARE FREQUENCY DEPENDENT (DATA SHOWN FOR AD9617 OP AMP)

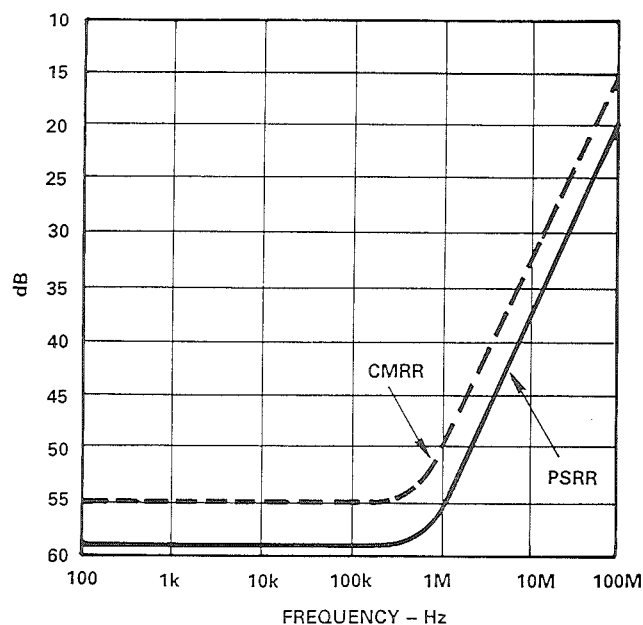


Figure 1.83

Power Supplies and Decoupling

It is because the PSRR of op amps is frequency dependent that op amp power supplies must be well decoupled. At low frequencies, several devices may share a 10 - 50 μ F capacitor on each supply, provided it is no more than 10cm (PC track distance) from any of them. At

high frequencies, each IC must have every supply decoupled by a low inductance 0.1 μ F (or so) capacitor with short leads and PC tracks. These capacitors must also provide a return path for HF currents in the op amp load. (See Reference 8).

PROPER LOW AND HIGH-FREQUENCY DECOUPLING TECHNIQUES FOR OP AMPS

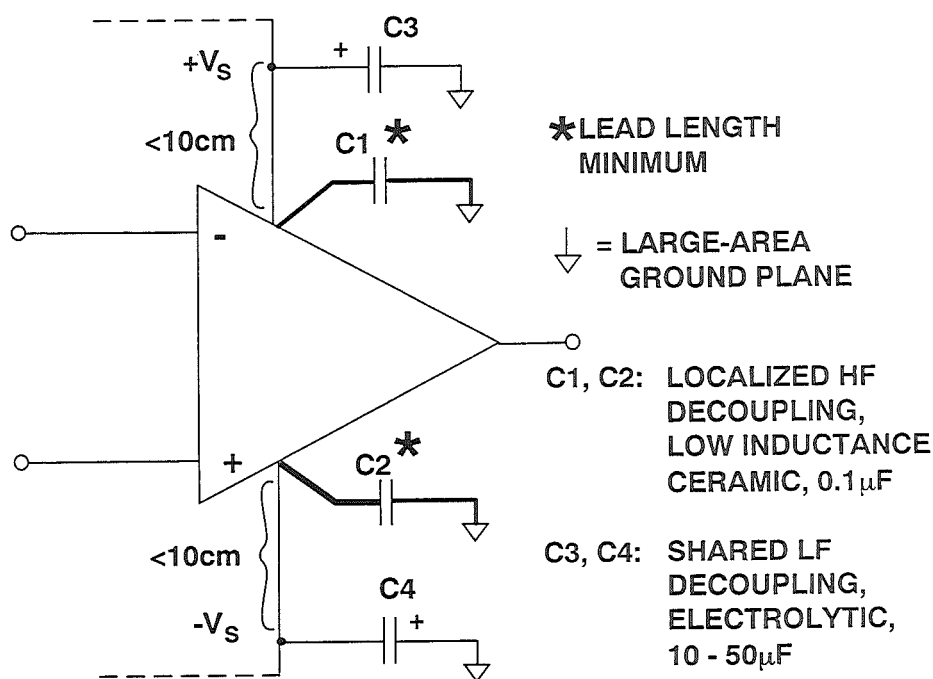


Figure 1.84

Power Supplies and Power Dissipation

Op amps have no ground terminal. Specifications of power supply are quite often in the form $\pm X$ Volts, but in fact it might equally be expressed as $2X$ Volts. What is important is where the common-mode range and output swings lie relative to the supplies. This information may be provided in tabular form or as a graph. Graphs are usually more informative, but tables containing minima and maxima make worst case design easier.

Often data sheets will advise that an op amp will work over a range of supplies (from +3 to ± 16.5 V for example), and will then give parameters at several values of supply, so that users may extrapolate between them. If the minimum supply is quite high, it is usually because the device contains some structure which requires high voltage to function (a zener diode, for instance).

POWER SUPPLIES

- Op Amp supplies can vary from +1.5V to ± 25 V
- Do not use an Op Amp outside the specified supply range
- Most data sheets show how performance varies with supply
- Every op amp should have its supply pins well decoupled at HF

Figure 1.85

Data sheets also give current consumption. Any current flowing into one supply pin will flow out of the other or out of the output terminal. When the output is open circuit, the dissipation is easily calculated from the supply voltage and current. When current flows in a load, it is easiest to calculate the total dissipation (remember that if the load is grounded to the center rail the load current flows from a supply to ground,

not between supplies), and then subtract the load dissipation to obtain the device dissipation.

The data sheet will normally give details of thermal resistances θ_{ja} (junction-to-ambient), θ_{jc} (junction-to-case), and maximum junction temperature ratings, from which dissipation limits may be calculated knowing ambient or case temperatures.

OP AMP POWER DISSIPATION

- Fast op amps run hot and may require heat sinks
- Calculate no-load dissipation from the data sheet values
- Calculate total power dissipation (including the load)
- Subtract the load dissipation
- Check that the remaining total is within permitted limits
- Use θ_{ja} and/or θ_{jc} to calculate maximum operating junction temperature and check that it is within limits

Figure 1.86

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